

MODEL NAME : AAZ50

PCB NO : DAA0009W000

BOM P/N :

GPIO MAP: Gen7 GPIO Master_1127

Beaver Creek 12" UMA

Skylake U

2015-09-23

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

TCM@ : TPM & China TPM select

MB PCB

Part Number	Description
DA21DK00100	PCB AAZ50 LA-C451P LS-C451P 02

Layout Dell logo



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REV: A00
PWB:

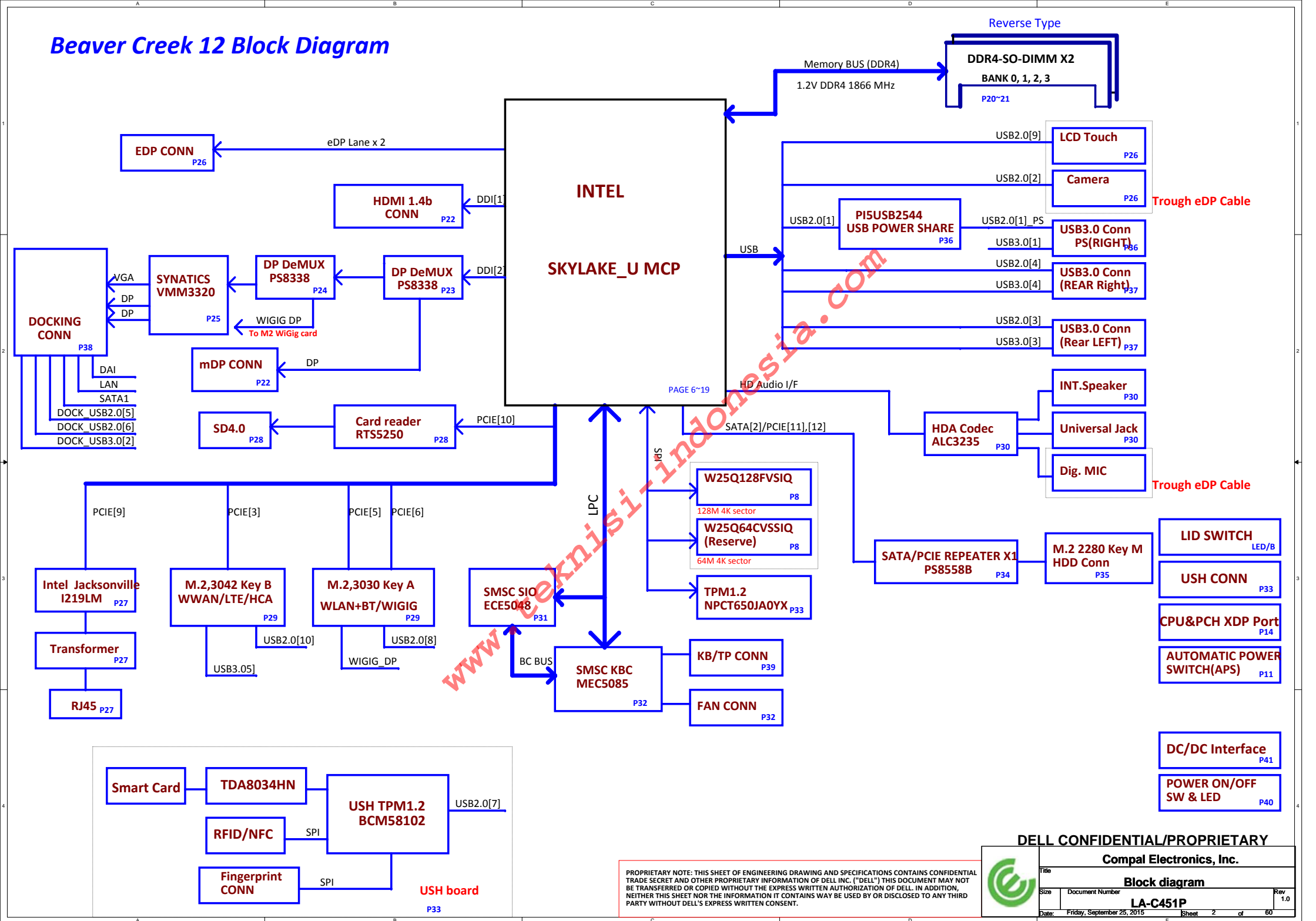
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Beaver Creek 12 Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	power plane	(M-OFF)
S0	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S3	ON	ON
S5 S4/AC	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF

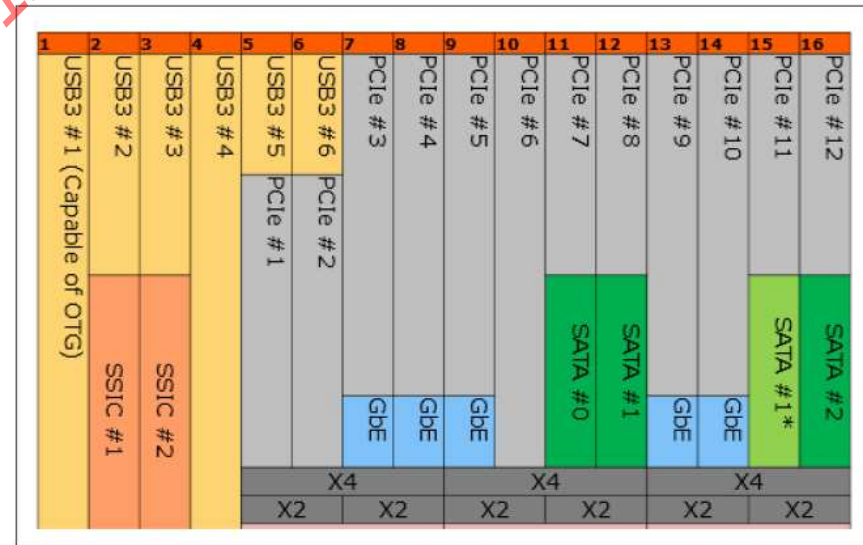
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	NP-155F	0.50
			Add Plating		
1	Top	3.7	Copper foil	0.5+plating	1.80
2	GND/PWR	3.8	Prepreg	1080	2.65
3	IN 1	3.7	Copper foil	0.5oz	0.65
4	GND/PWR	3.8	Core	4mil	4.00
5	IN 2	3.7	Copper foil	0.5oz	0.65
6	IN 3	3.8	Prepreg	2112	3.95
7	GND/PWR	3.7	Copper foil	0.5 oz	0.65
8	IN 4	3.8	Core	4mil	4.00
9	GND/PWR	3.7	Copper foil	0.5 oz	0.65
10	Bottom	3.8	Prepreg	1080	2.65
			Add Plating		
			SolderMask	NP-155F	0.50
Overall Thickness (1.0mm ± 10%)				39.37	40.81000 1.036574

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right
USB3.0-2	SSIC-1			EDOCK PORT1
USB3.0-3	SSIC-2			JUSB1-->Rear Left
USB3.0-4				JUSB2-->Rear Right
USB3.0-5		PCIE-1		M2 3042(WWAN)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3042(HCA or QCA LTE)
		PCIE-4		NA
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	EDOCK E-SATA
		PCIE-9		LOM
		PCIE-10		Card Reader
		PCIE-11	SATA-1*	M.2 2280 SSD(Reverse) (PCIex2 or SATA)
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	Camera
3	JUSB2-->Rear Left
4	JUSB3-->Rear Right
5	EDOCK PORT1
6	EDOCK PORT2
7	USH
8	M.2 304230(BT)
9	Touch Screen
10	M2 3042(WWAN)

USH	H	BIO
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High Speed I/O (HSIO) Lane Multiplexing in SKL U



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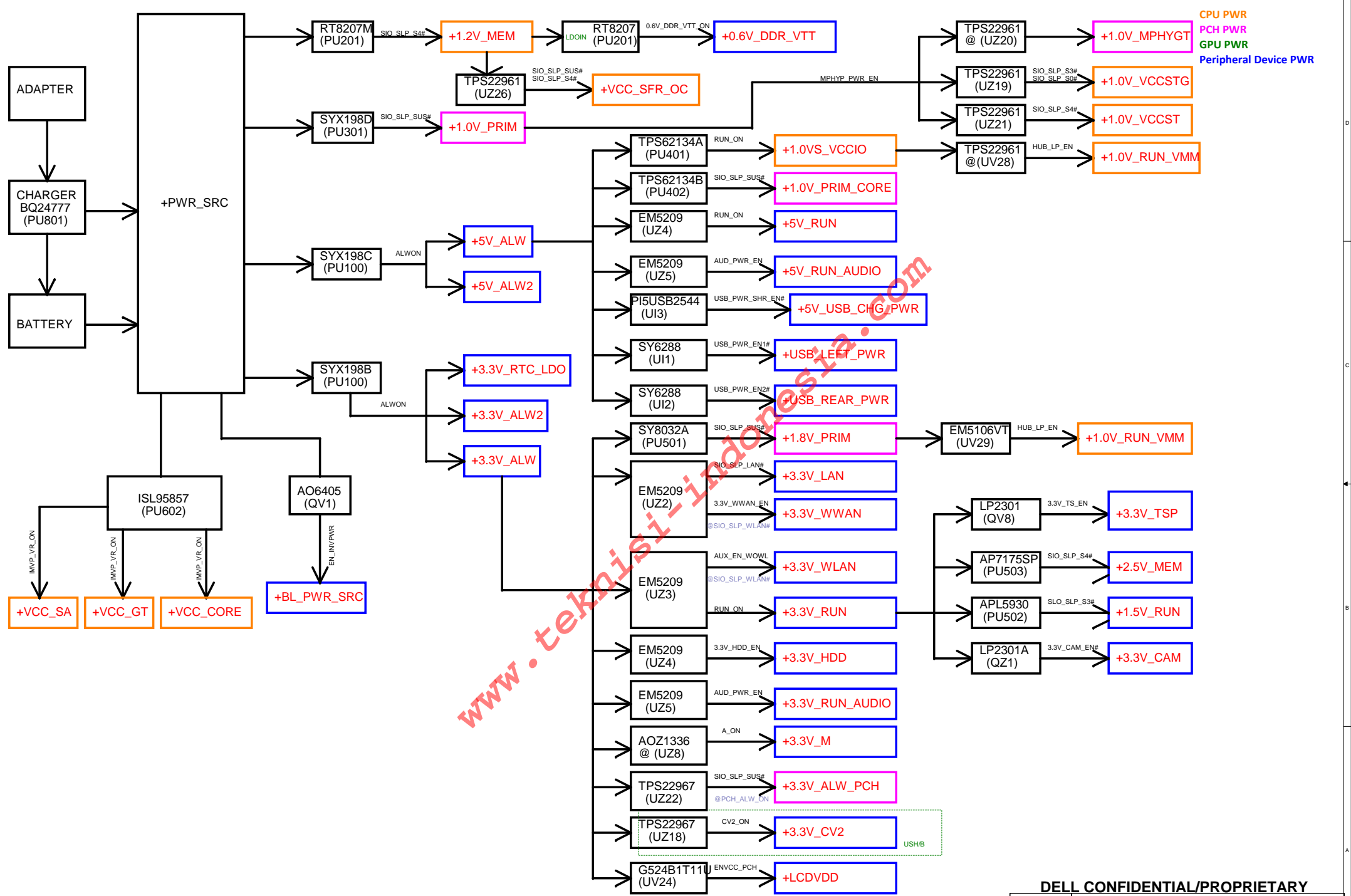


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Port assignment

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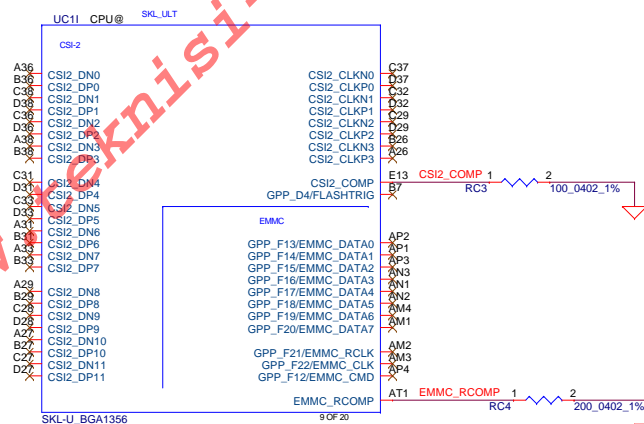
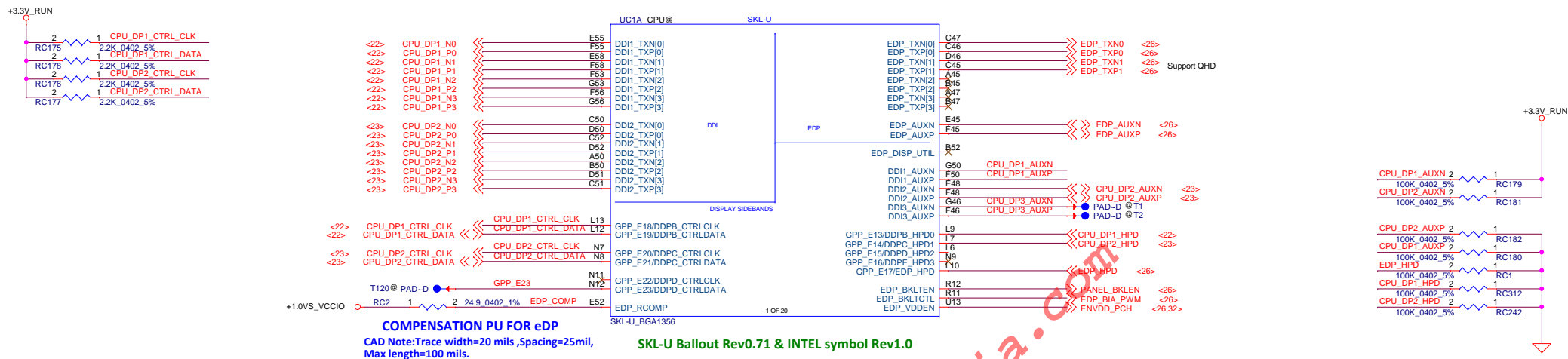


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Power rails
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**CPU (1/14)**

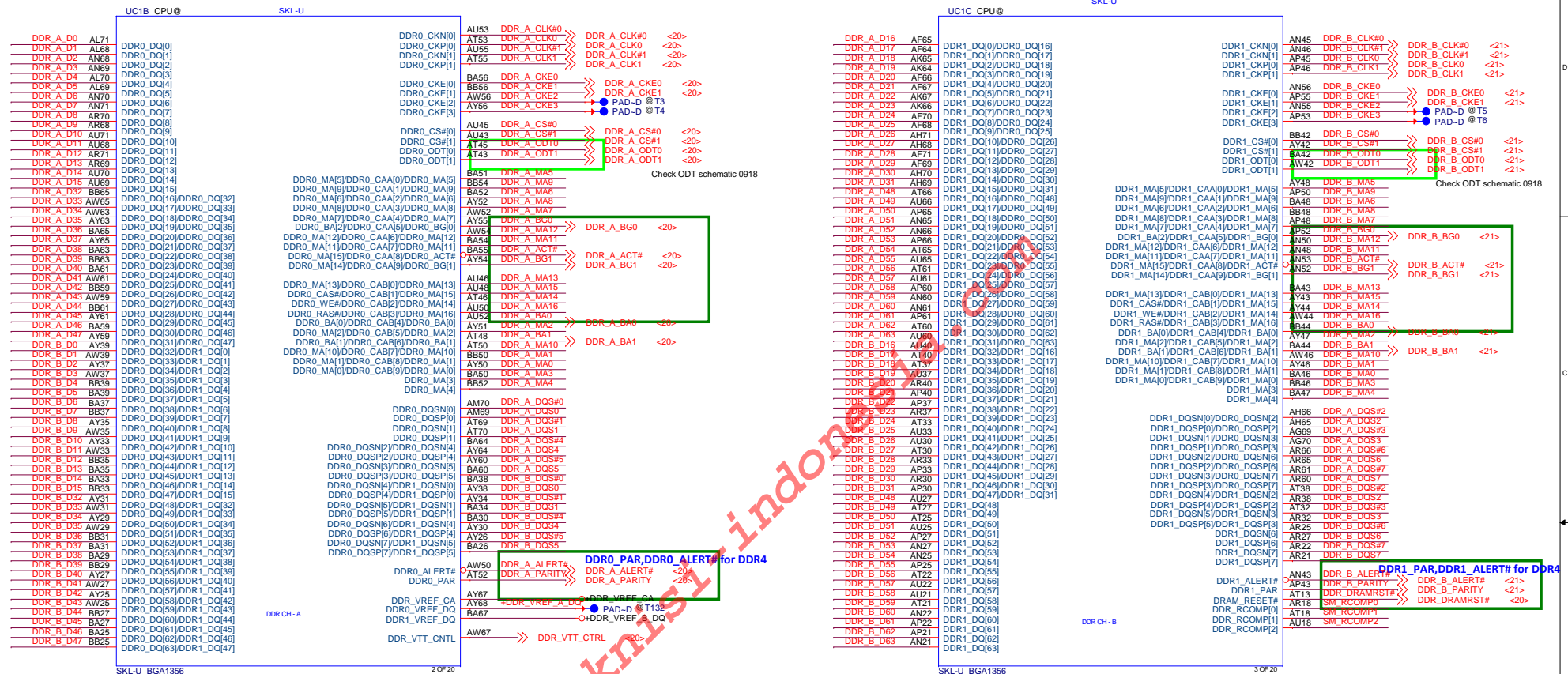
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DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



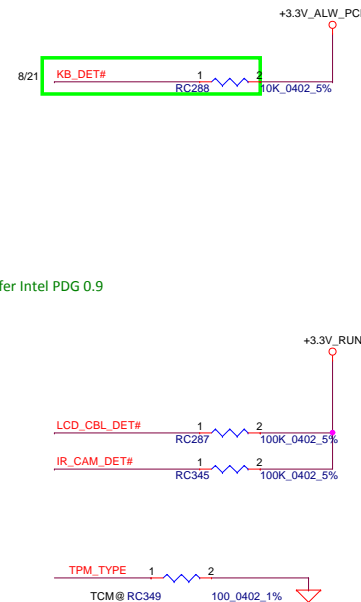
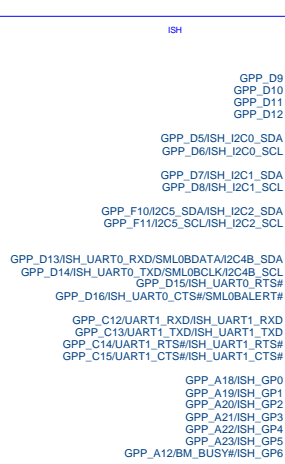
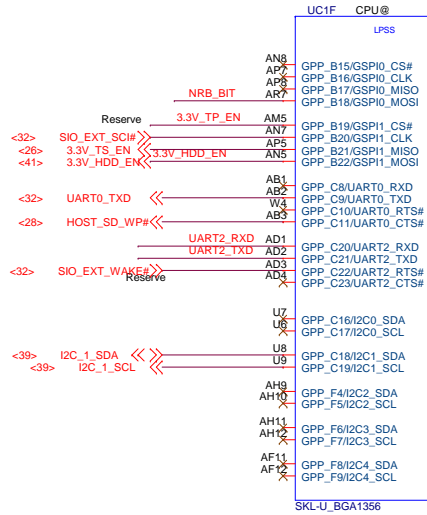
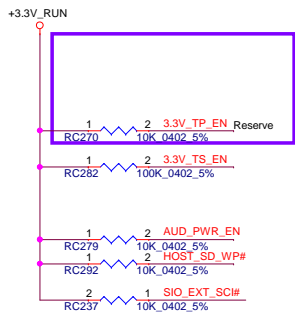
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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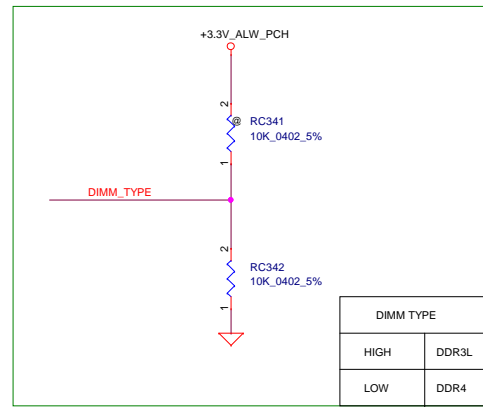
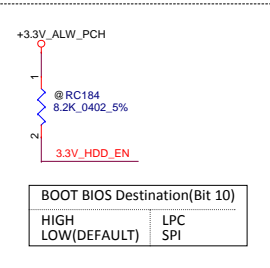
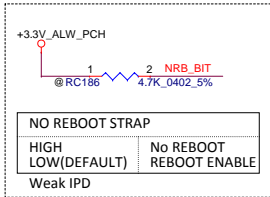
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RC349	
POP	China TPM
DEPOP	TPM



DIMM TYPE	
HIGH	DDR3L
LOW	DDR4

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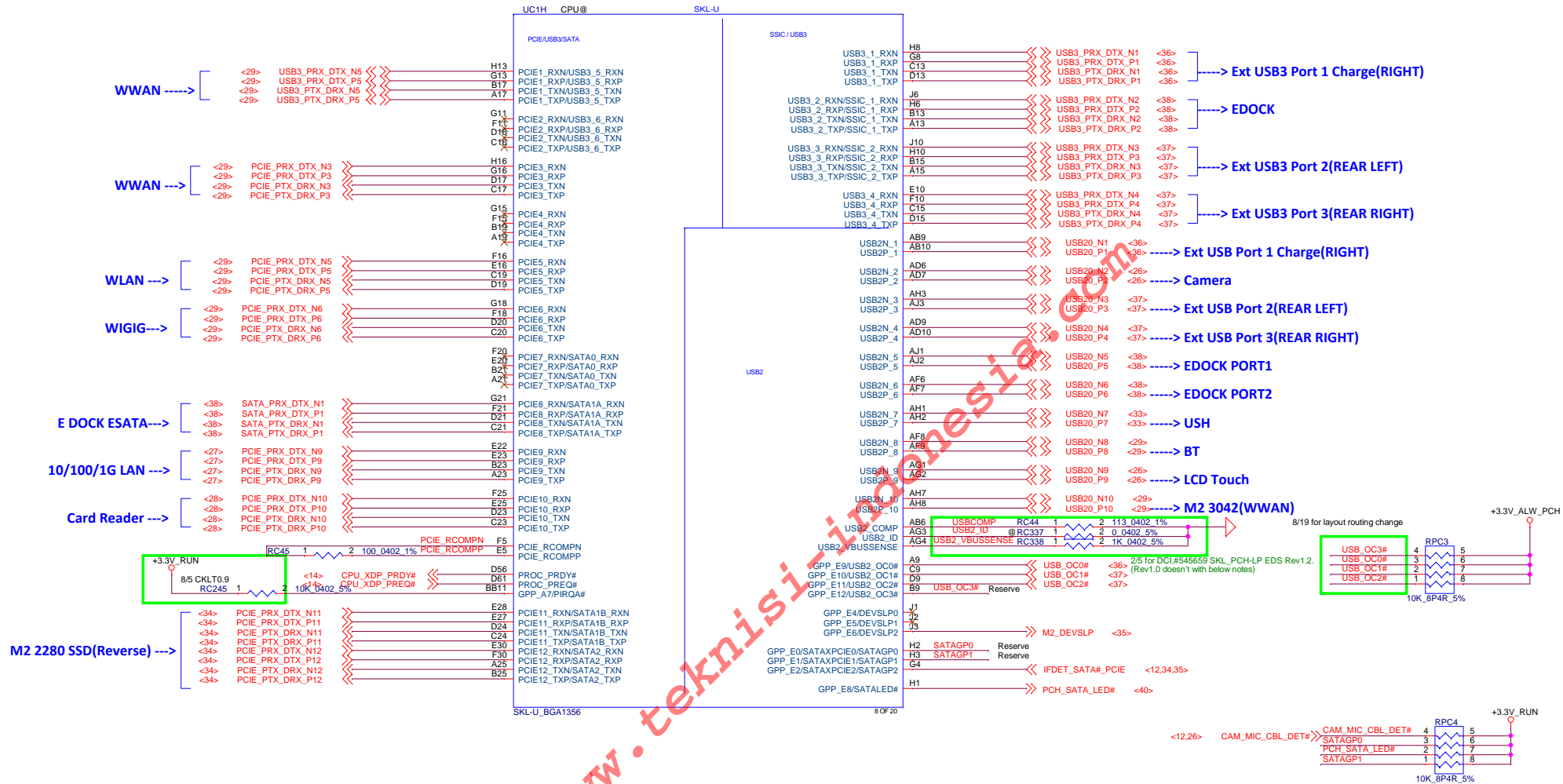
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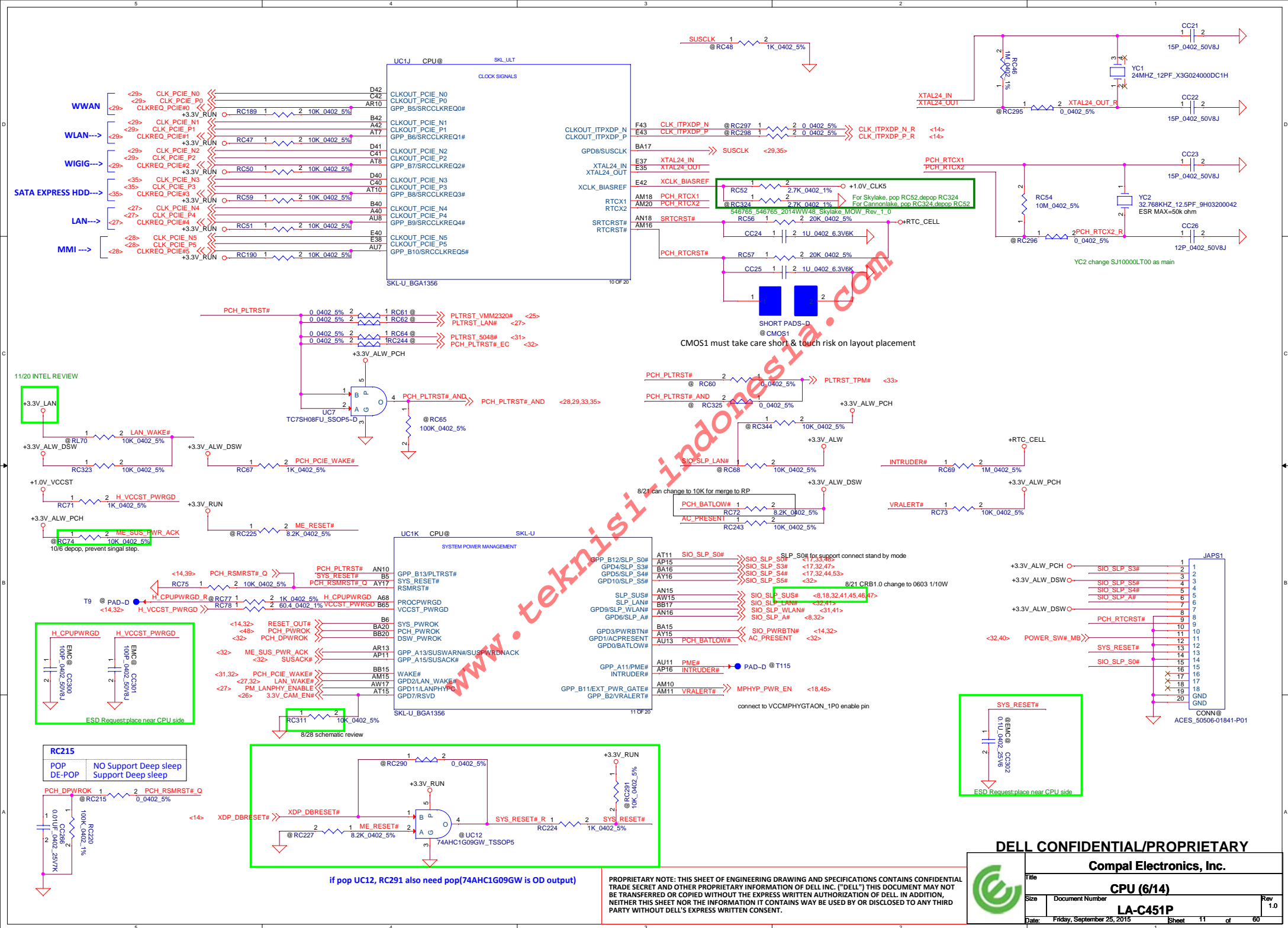
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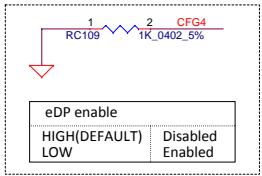
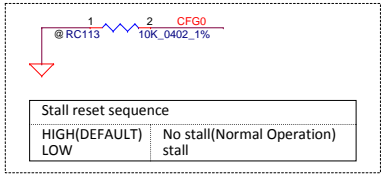
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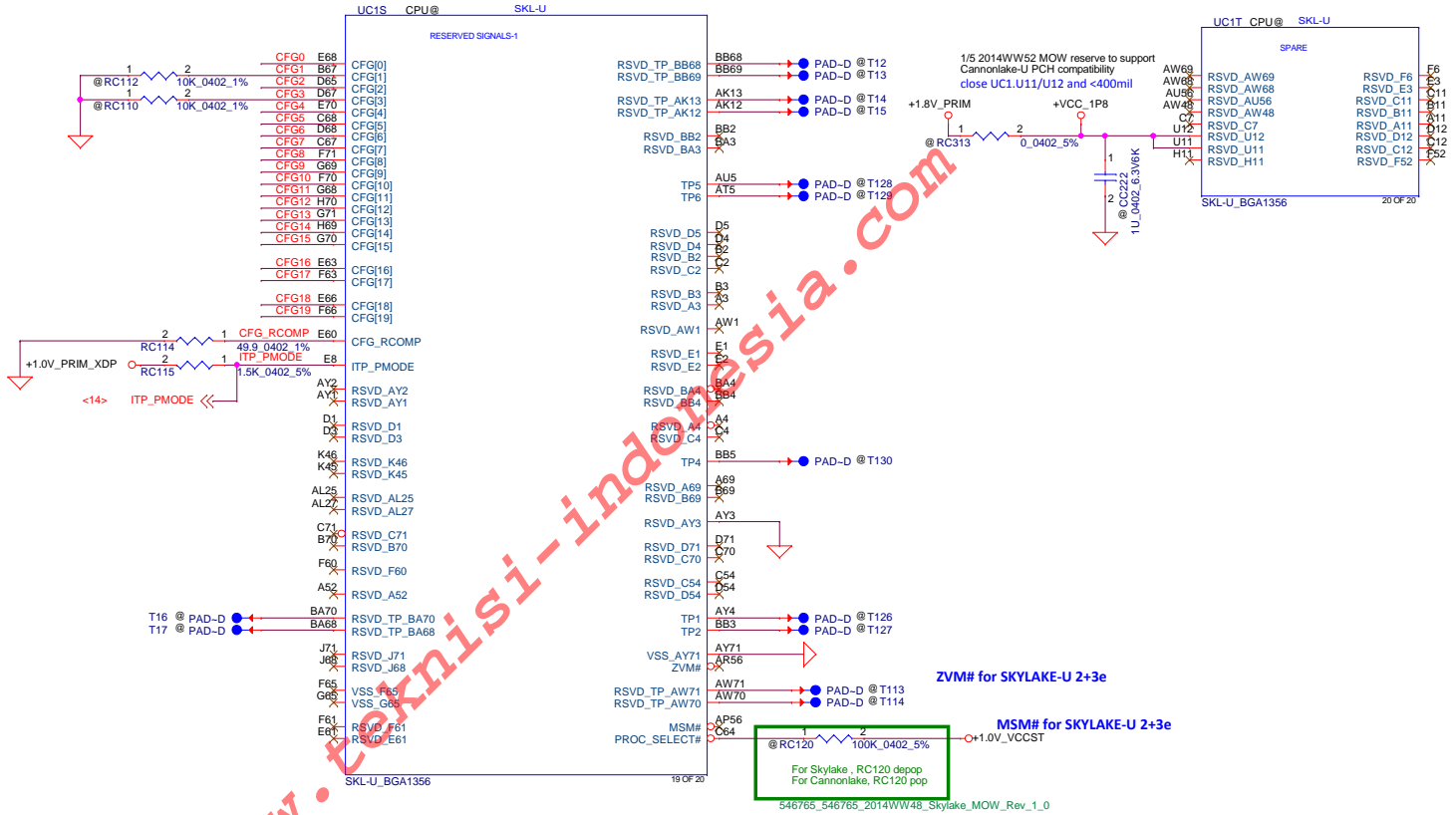
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CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



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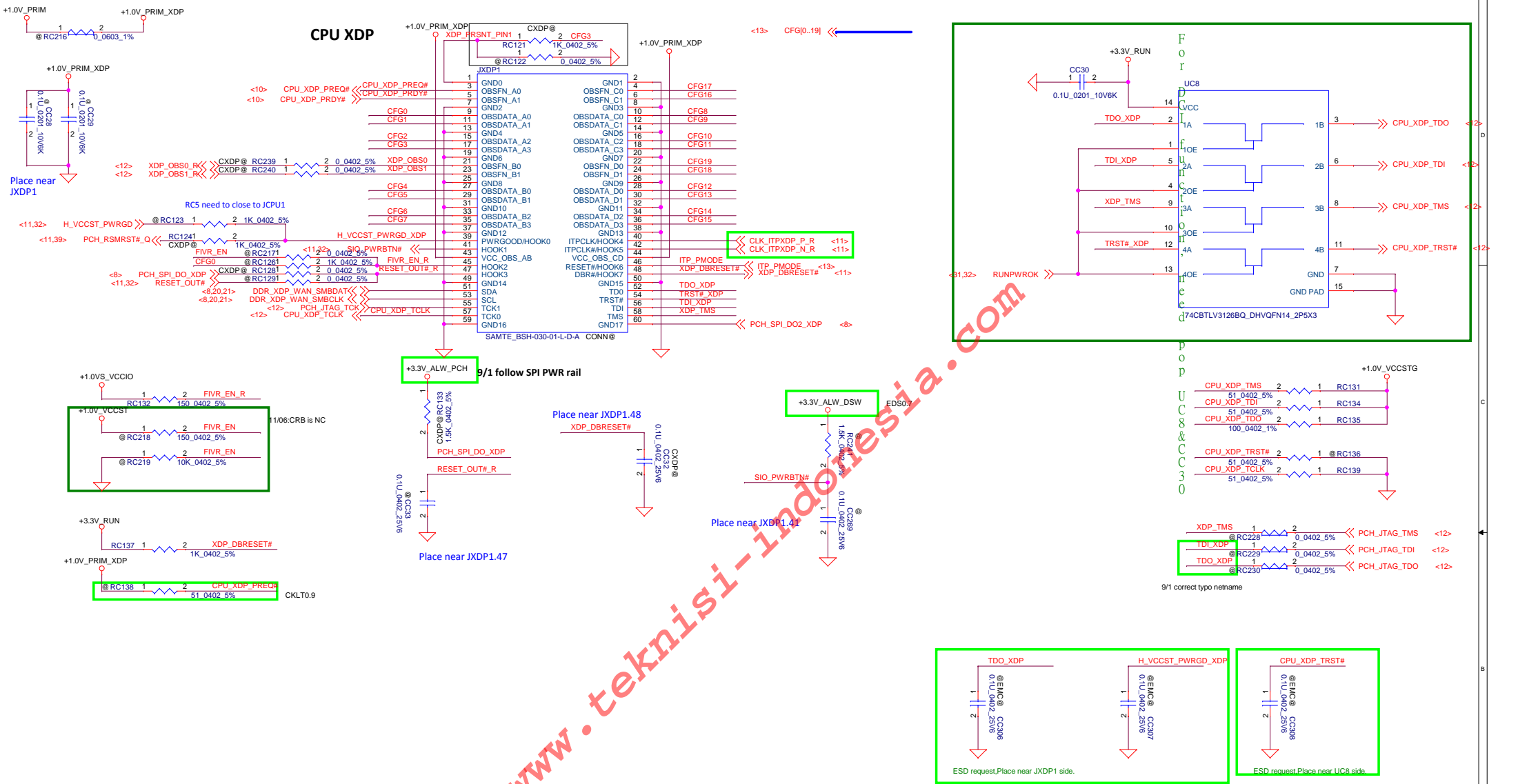
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CPU (8/14)

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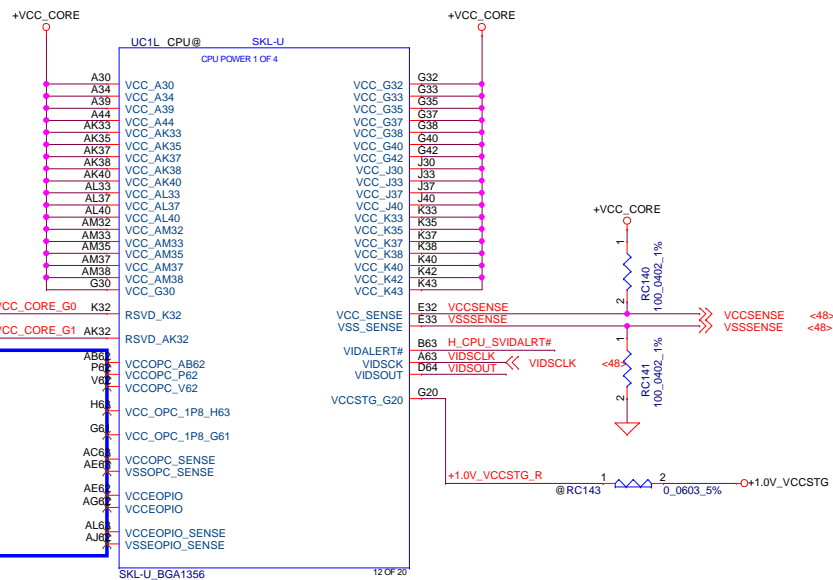
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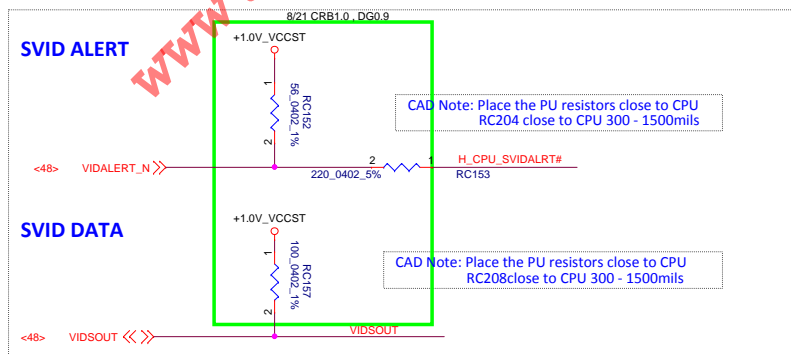
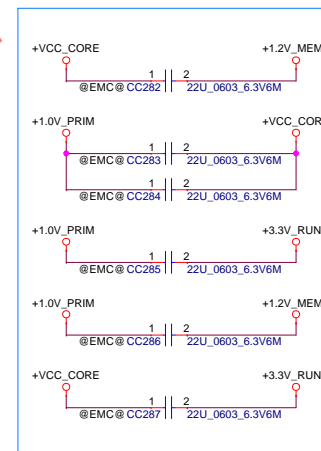
+VCC_CORE: 0.3~1.35V



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Power source

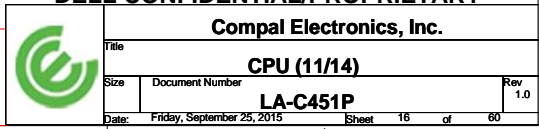
ESD Request



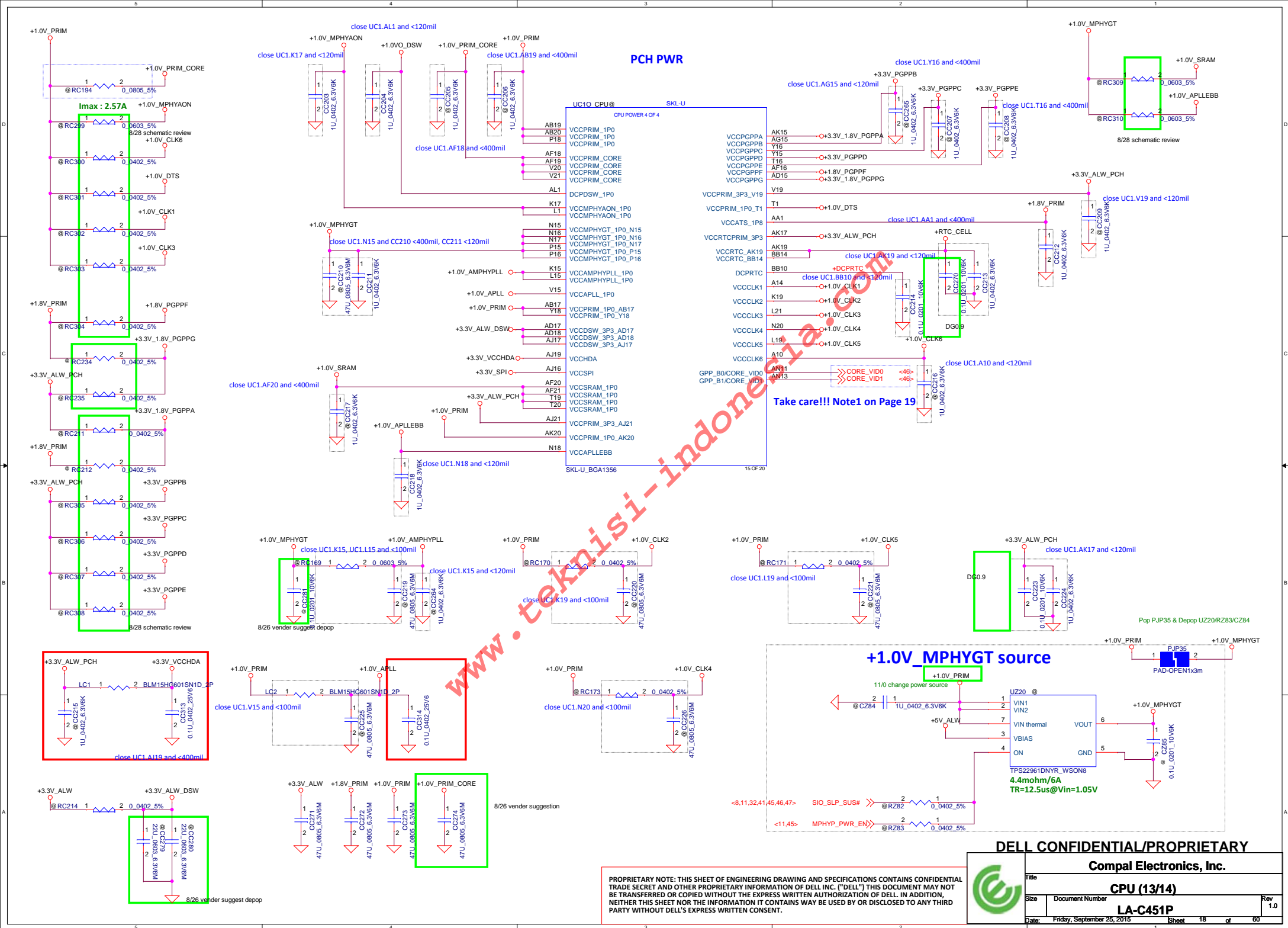
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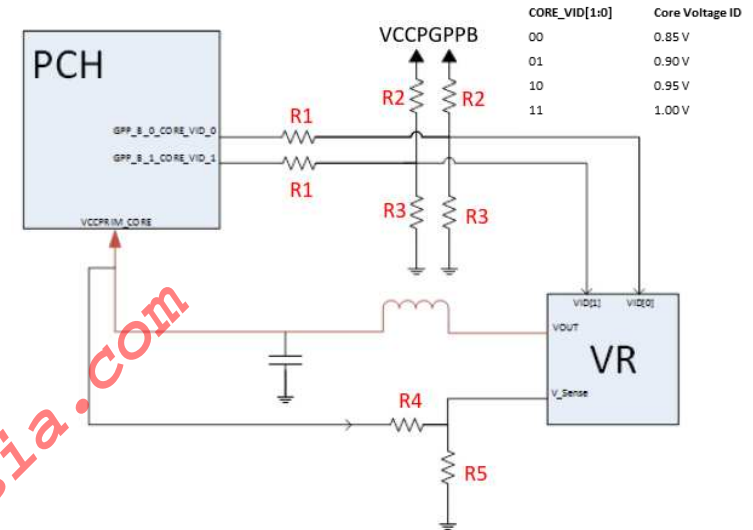


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Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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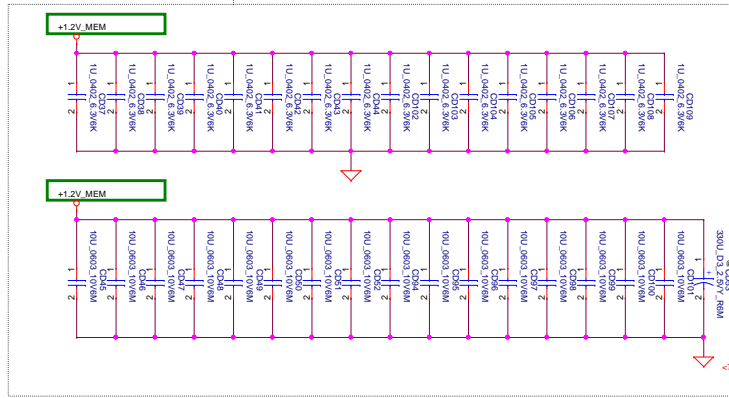


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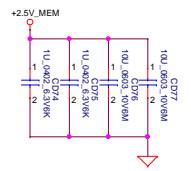
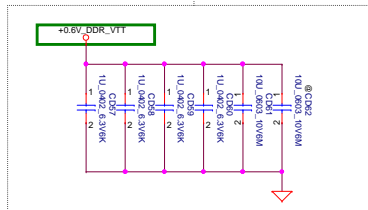
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<7> DDR_B_DQS[0..7] <<>>
 <7> DDR_B_D[0..63] <<>>
 <7> DDR_B_DQS[0..7] <<>>
 <7> DDR_B_MA[0..16] <<>>

Layout Note:
Place near JDIMM2

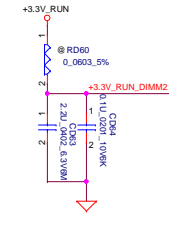
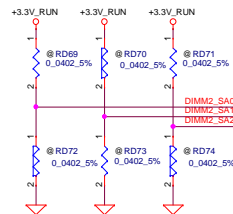


Layout Note:
Place near JDIMM2.203,204

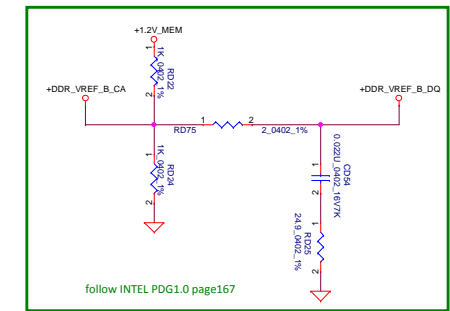
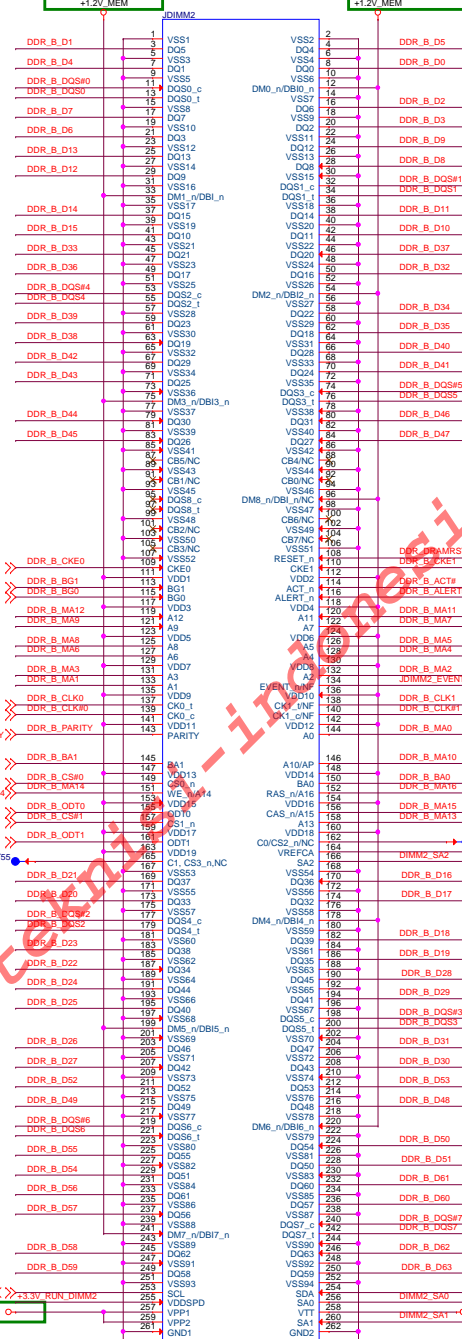


DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



JDIMM2 REV Type H=5.2



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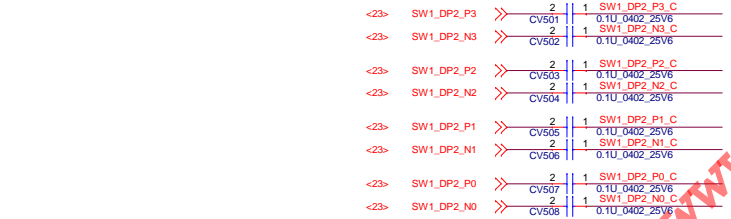
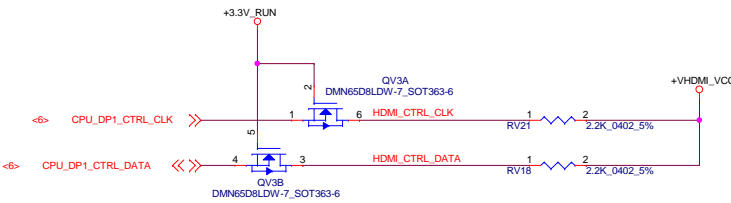
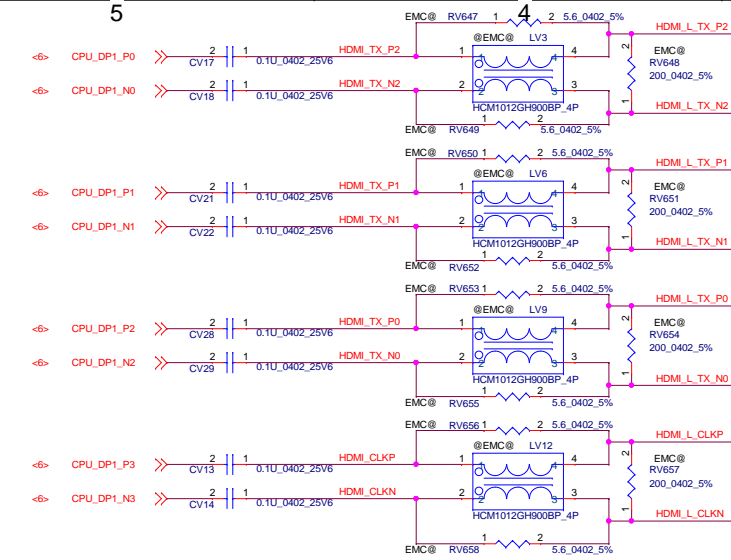
DDR4

LA-C451P

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LINK LOTES_ADDR0107-P005A DONE

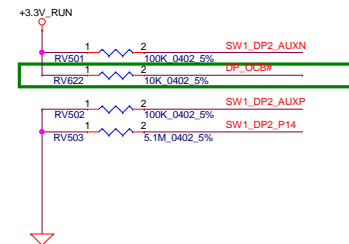
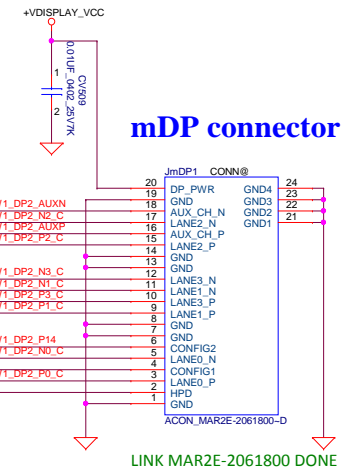
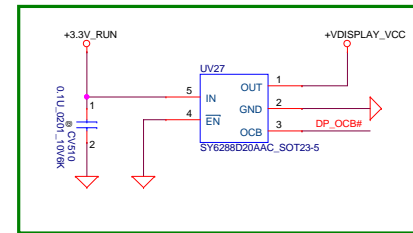
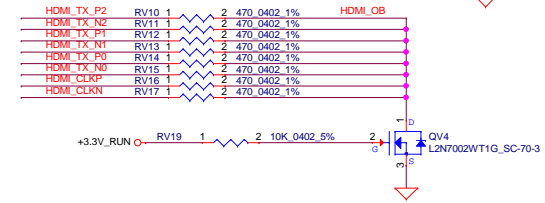
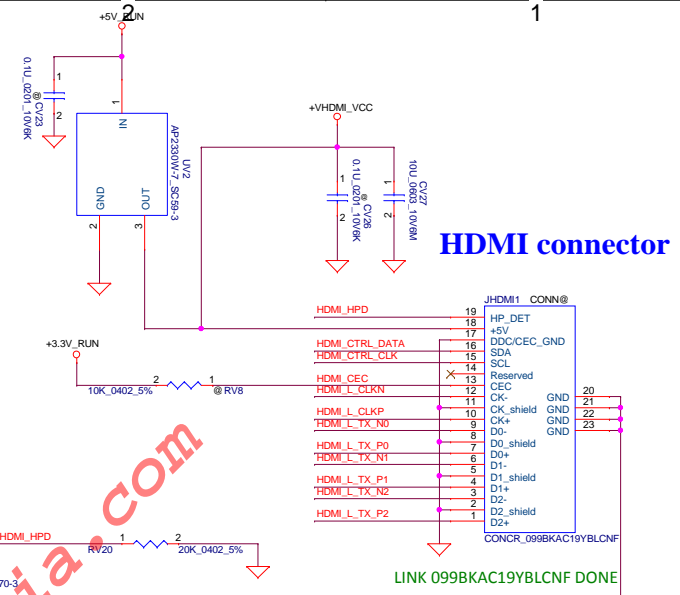
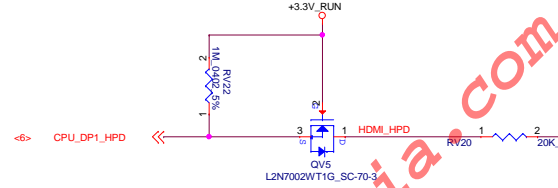
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9/29 vender request remove HPD Passgate Design

3

DFB request:
 main source:SM070003V00(INPAQ_HCM1012GH000BP)
 Footprint use 2nd source SM070004000(TAIYO_MCF12102G900-T_4P)
 Pitch change from 0.5mm to 0.55mm



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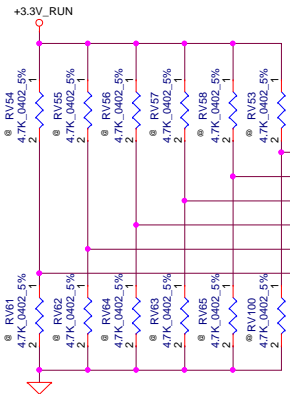
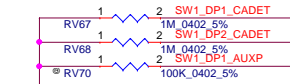
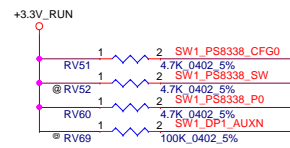
Compal Electronics, Inc.

HDMI CONN

LA-C451P

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 Date: Friday, September 25, 2015 Sheet 22 of 60

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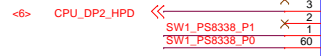
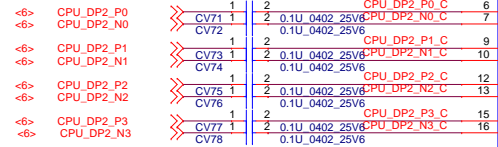
Port switching control or priority configuration. Internal pull down ~150Kohm, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

Vendor suggest MUX use LLEQ, PEQ=M and PIO=M

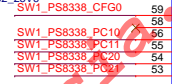
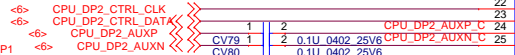
Programmable input equalization levels, Internal pull down at ~150Kohm, 3.3V I/O
PEQ =
L: default, LLEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M: LLEQ, compensate channel loss up to 8.5dB @HBR2

PIO: Automatic EQ enable, Internal pull down ~150K ohm, 3.3V I/O
PIO = L: Automatic EQ enable (default)
H: Automatic EQ disable

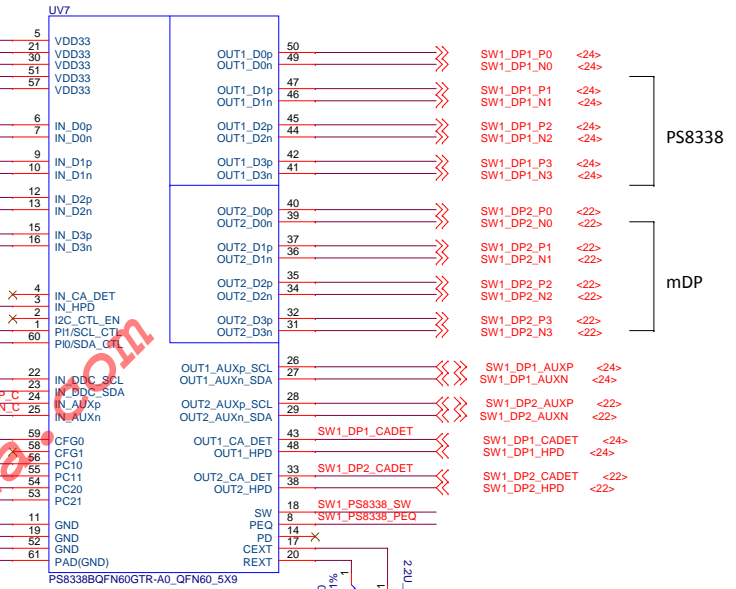
CV62 CV61 close to pin30 &57
CV66, CV69, CV70 close to pins 21,51



for support TMDS signal need contact SCL/SDA to P22,23



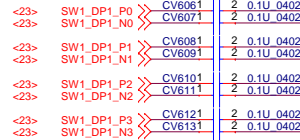
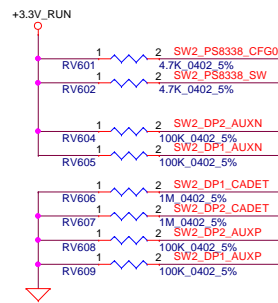
Dock has high priority when both ports plugged



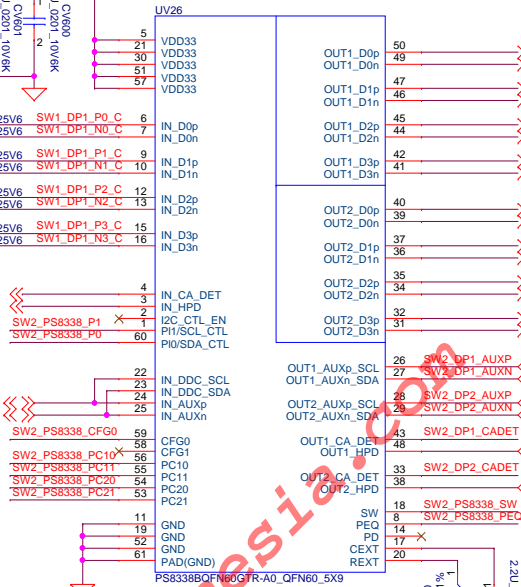
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Title DP SW			
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Date Friday, September 25, 2015		Sheet 23	of 60

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Dock has high priority when both ports plugged

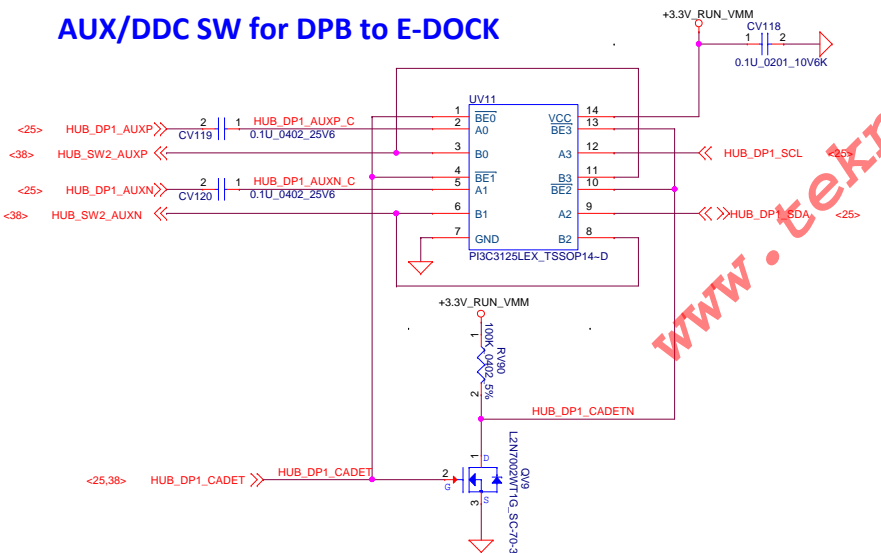


Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O

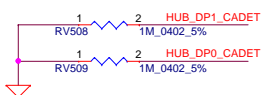
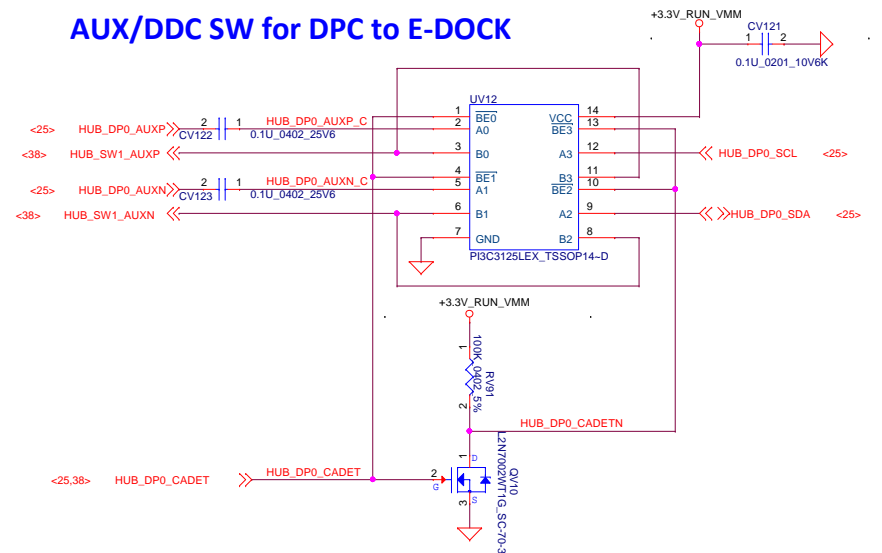
For Control Switching Mode (CFG0 = L):
 SW = L: Port1 is selected (default)
 SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H):
 SW = L: Port1 has higher priority when both ports are plugged (default)
 SW = H: Port2 has higher priority when both ports are plugged

AUX/DDC SW for DPB to E-DOCK



AUX/DDC SW for DPC to E-DOCK

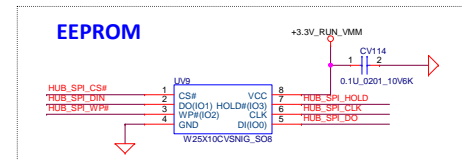
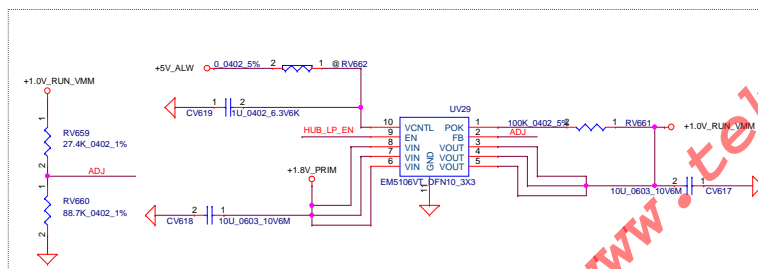
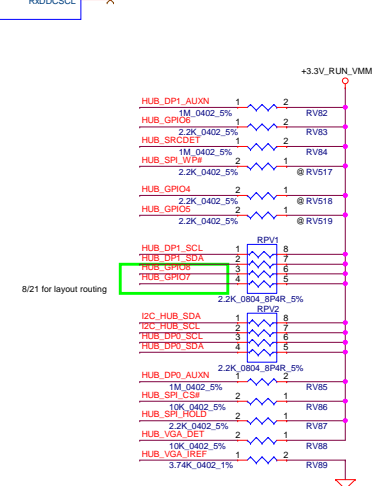
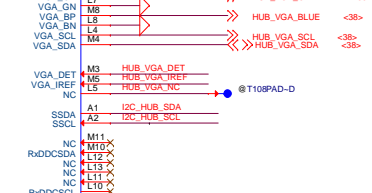
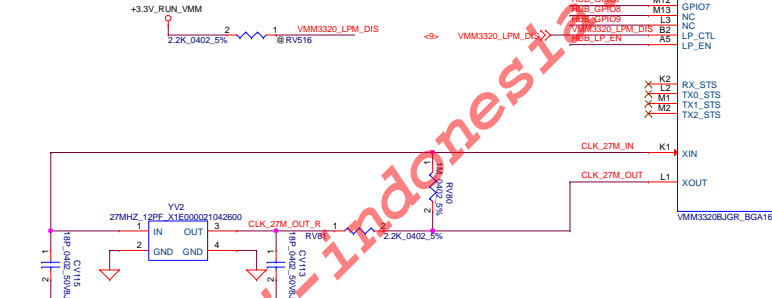
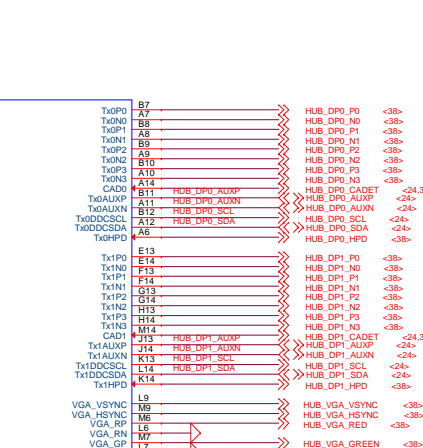
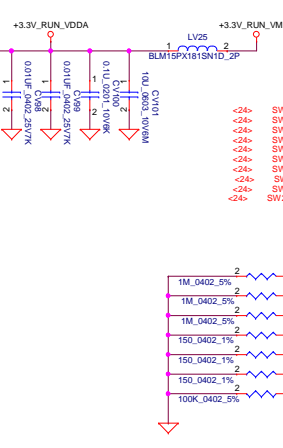


	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

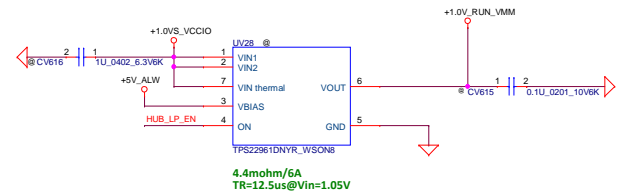
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Low Power Mode by external Load switch



VMM2320 Operation power consumption for 1.0V=1.464A (Max)

PRODUCT SUMMARY (SI3456DDV)			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
30	0.040 at V _{GS} = 10 V	6.3	2.8 nC
	0.050 at V _{GS} = 4.5 V	5.7	

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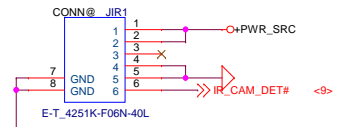
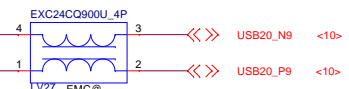
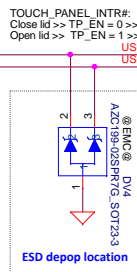
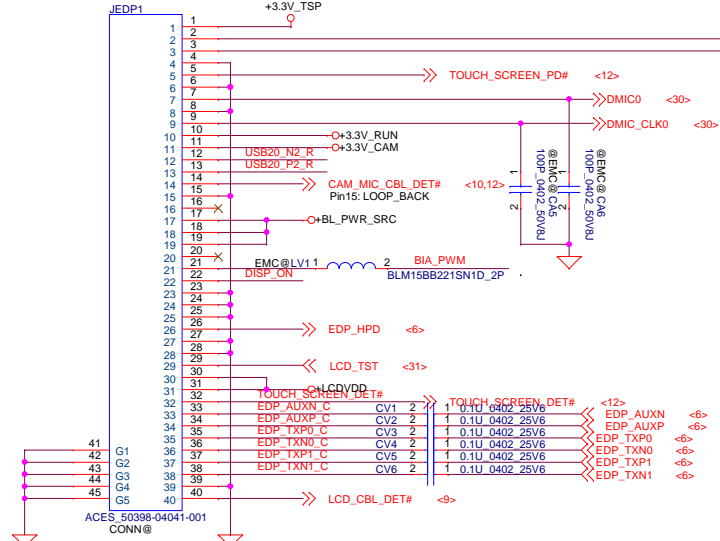
Compal Electronics, Inc.

DP 1.2 MST HUB

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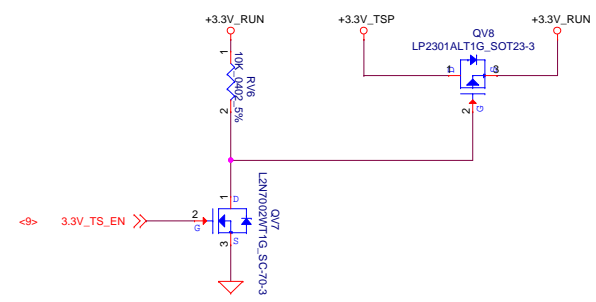
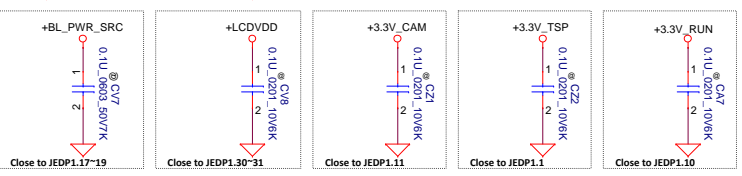
LINK 50398-04041-001 DONE



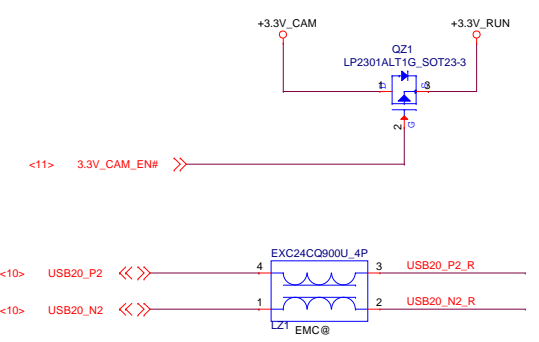
Due to BC12/14, PC12 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table

Link SP01001Y000 done

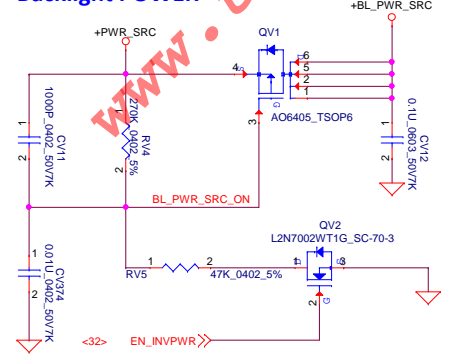
For Touchscreen



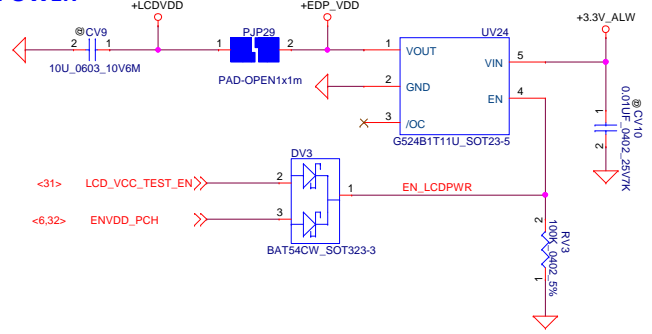
WebCAM



Backlight POWER



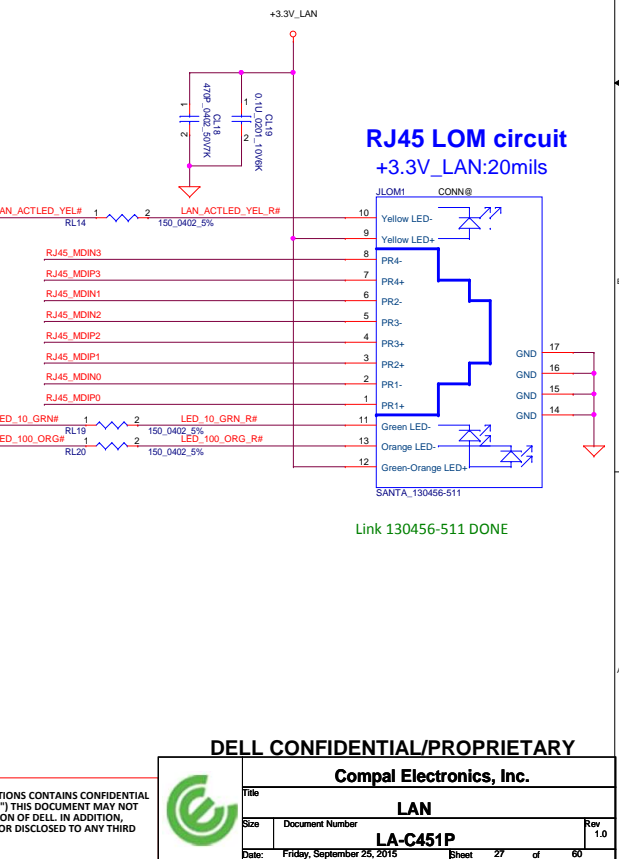
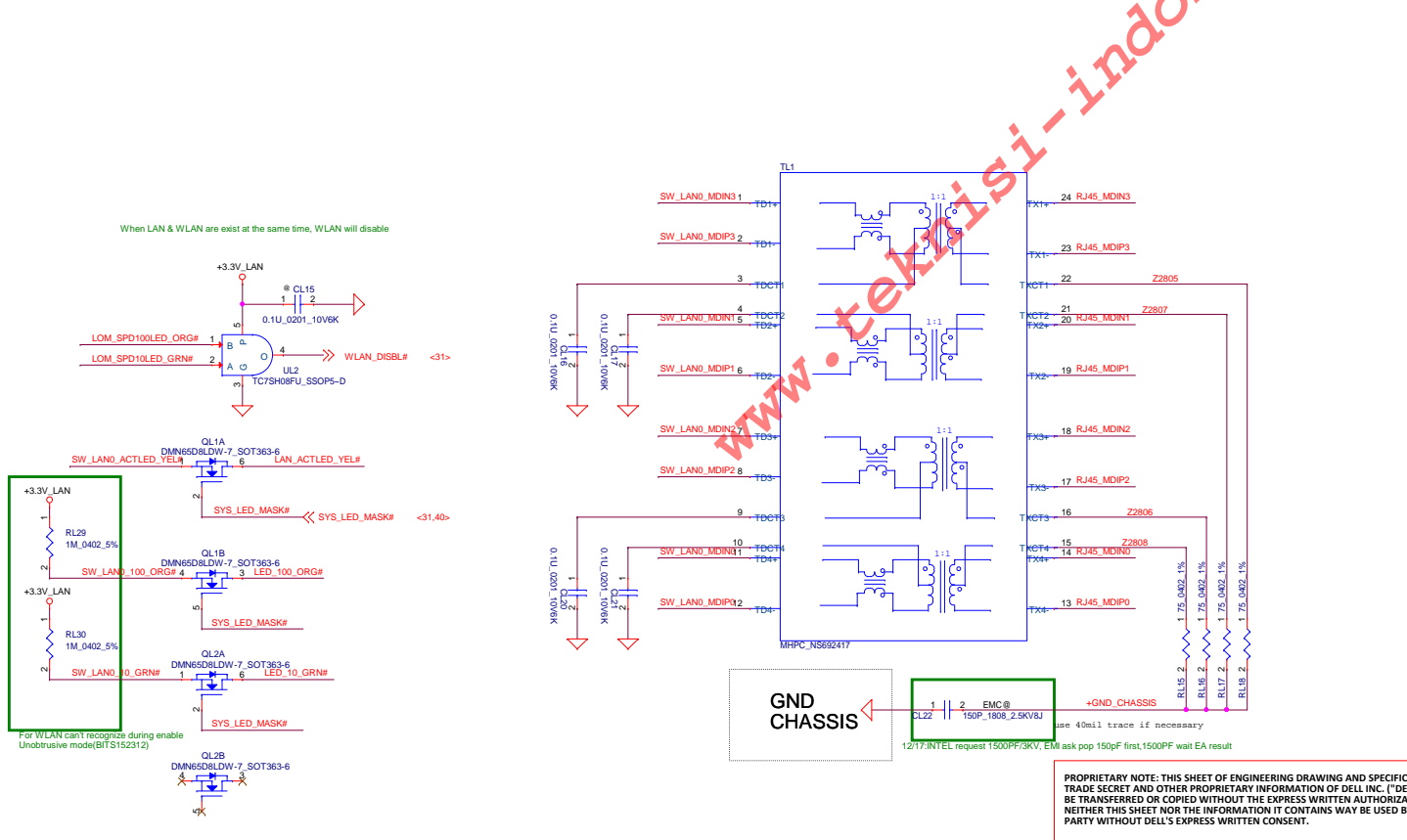
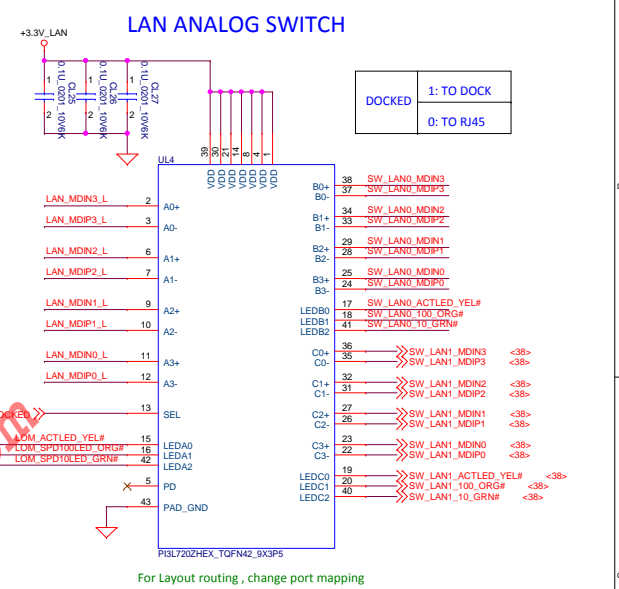
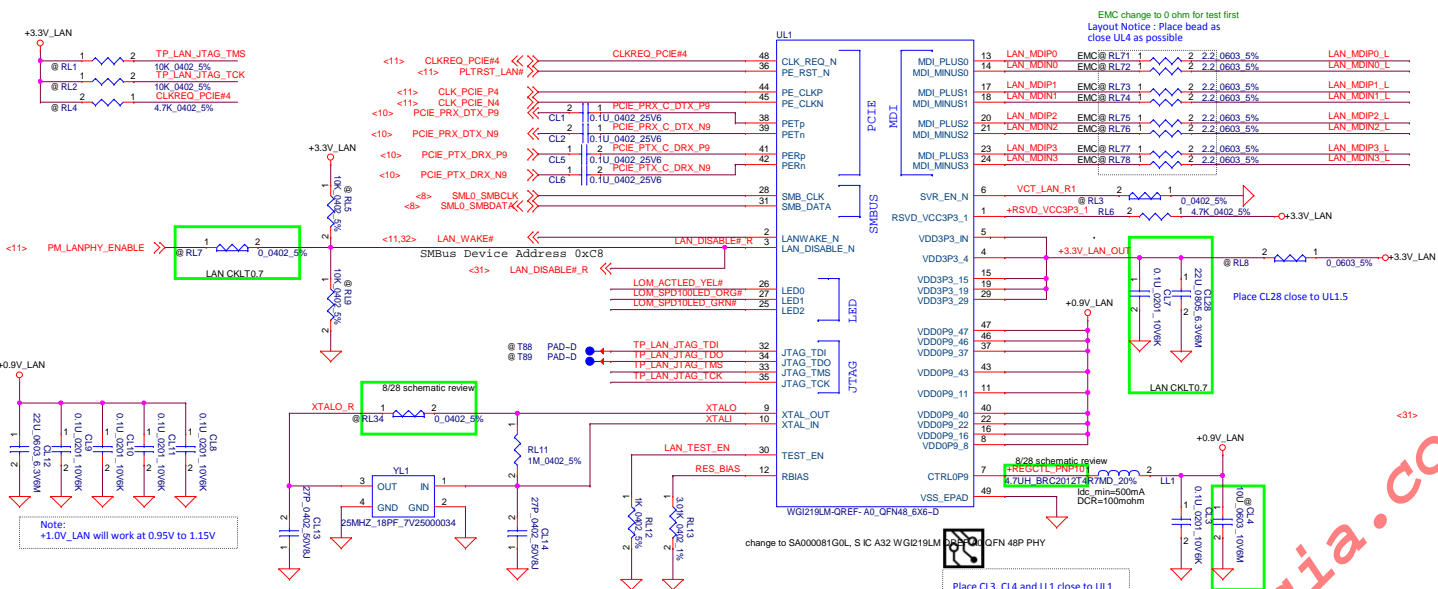
LCDVDD POWER

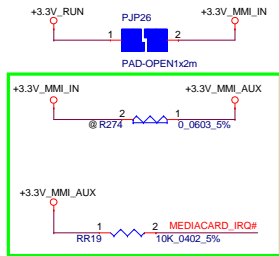


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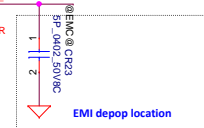
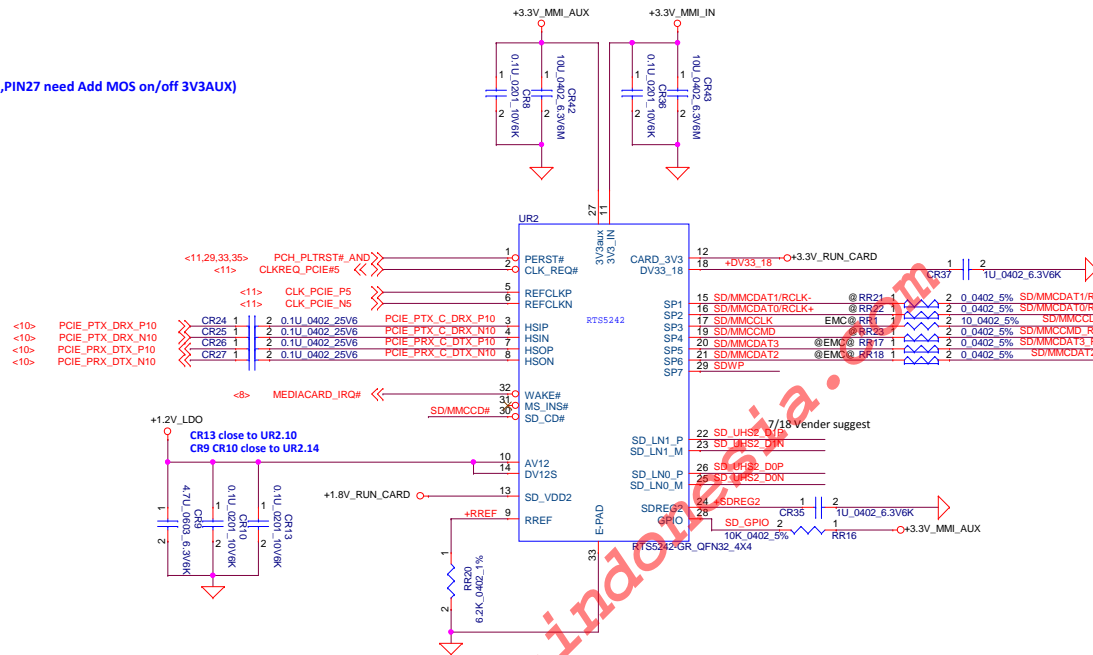
Compal Electronics, Inc.			
eDP CONN & Touch screen			
LA-C451P			
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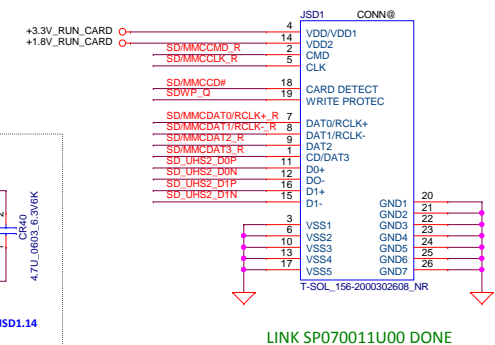
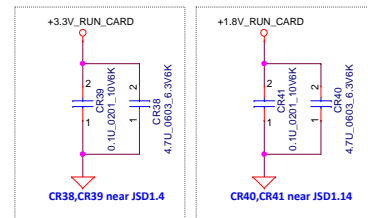
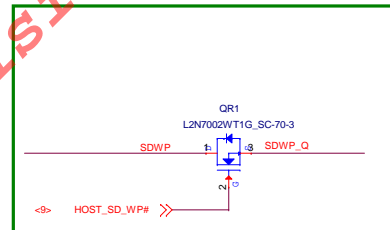


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
High	Low	Low	Write Enable
Low	High	High	Write Protect(SD&FW LOCK)
Low	Low	High	Write Protect(FW LOCK)



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Card Reader

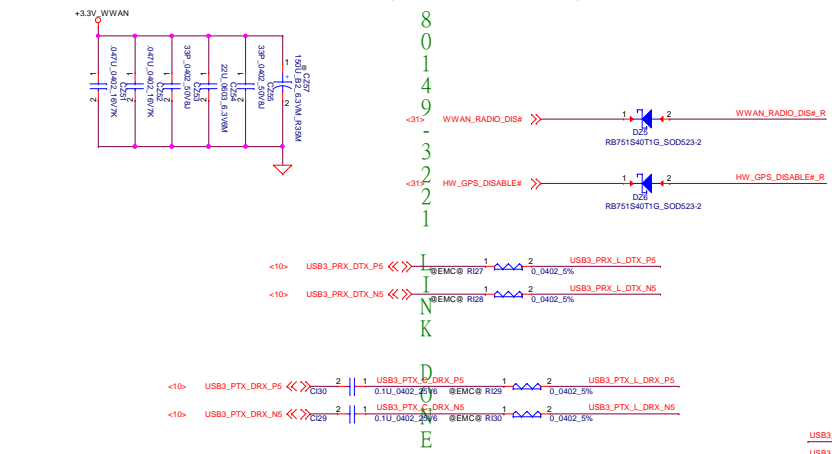
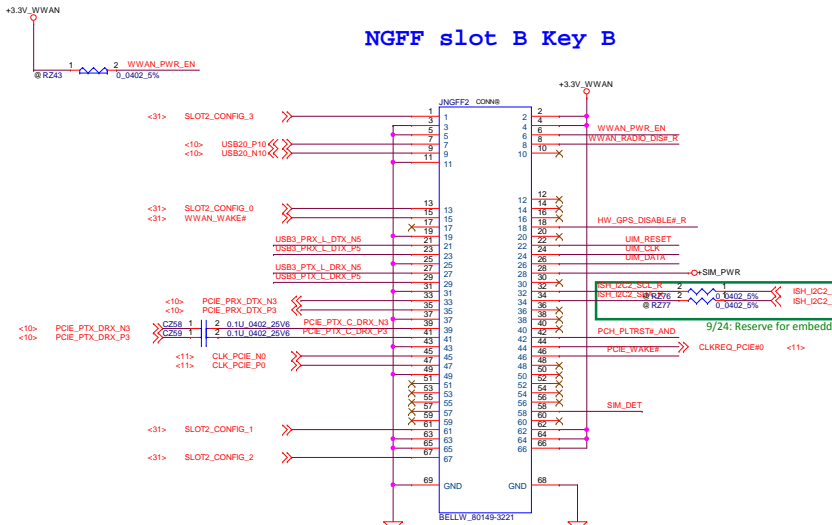
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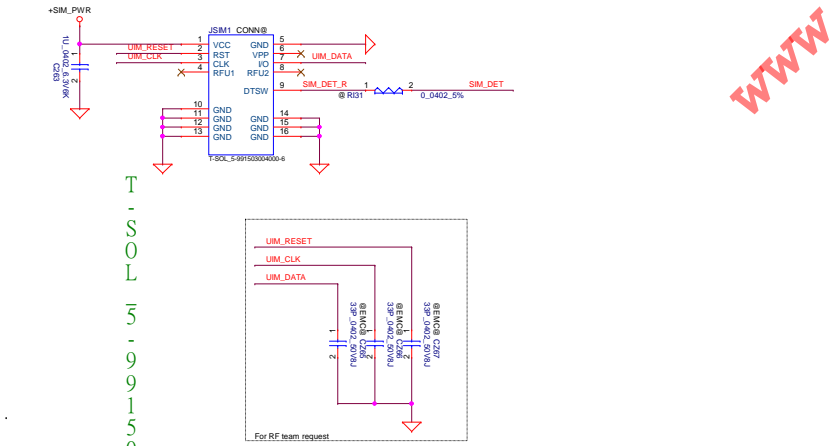


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NGFF slot B Key B

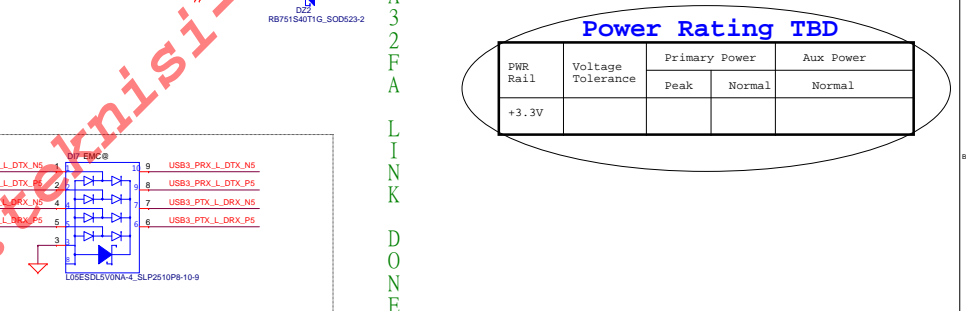
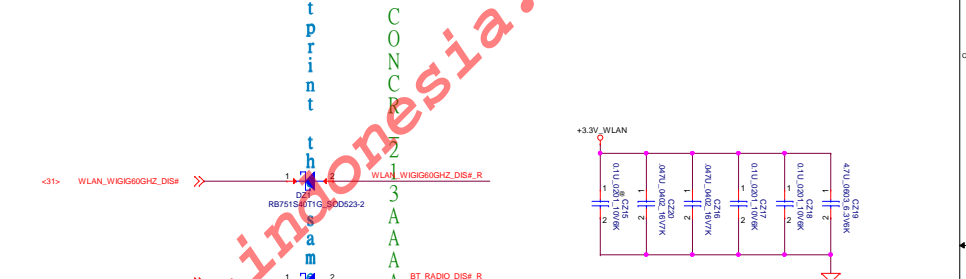
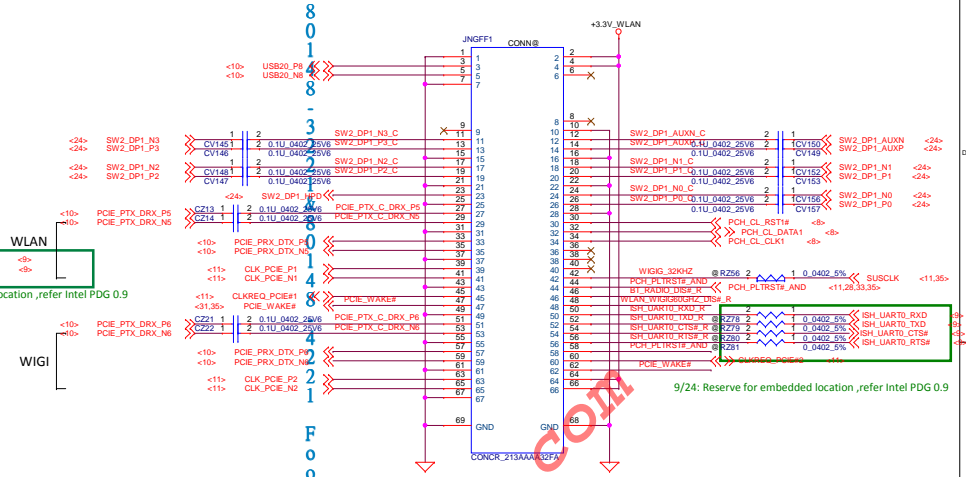


SIM Card Push-Push



T-SOL 5-991503030

NGFF slot A Key A



www.technisi-indonesia.com

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

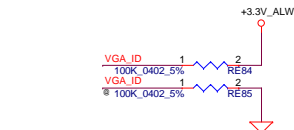
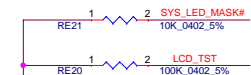
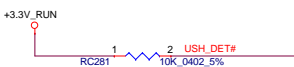
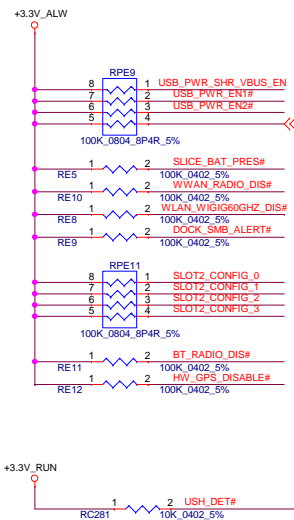
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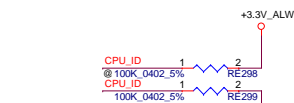


File	NGFF Card		
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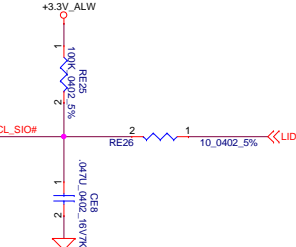
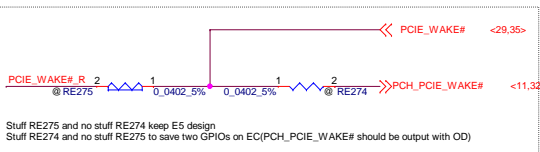
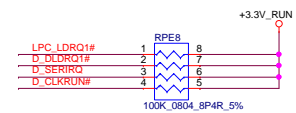
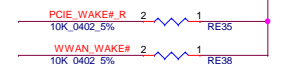
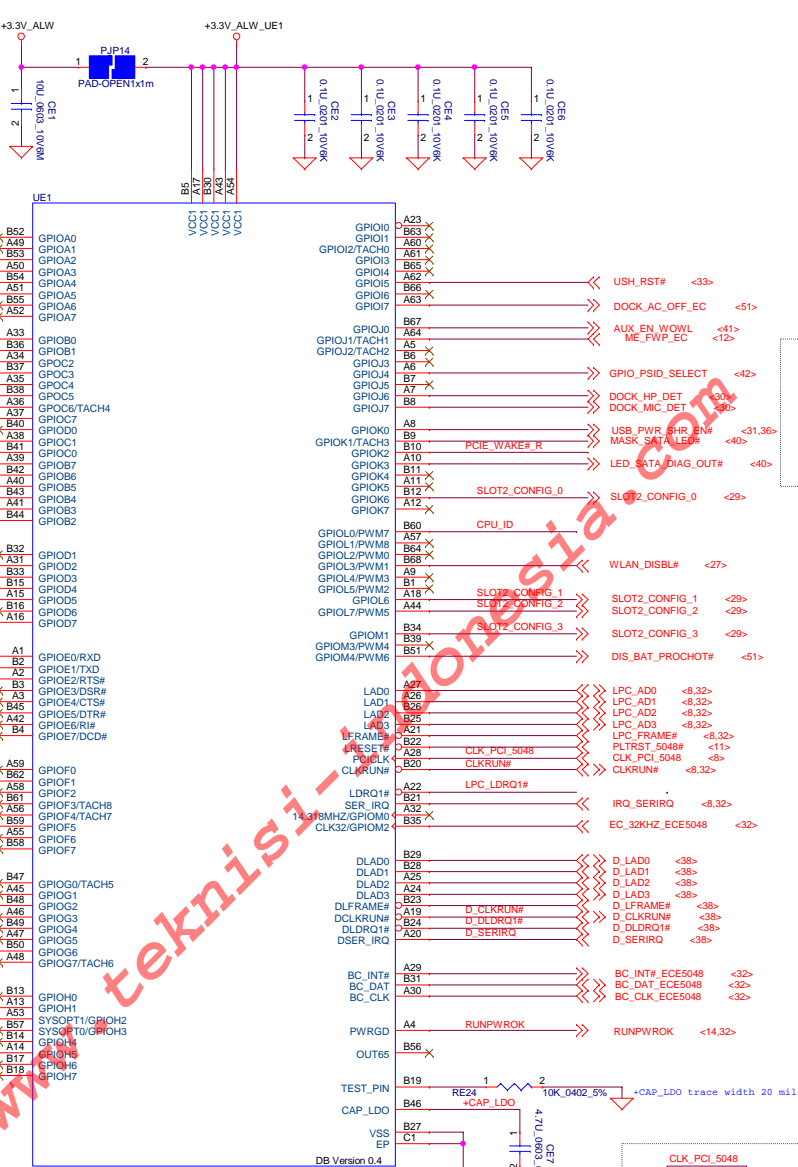
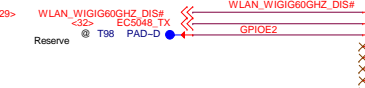
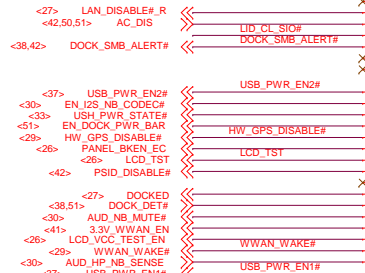
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	VGA_ID0
Discrete	0
UMA	1



	CPU_ID0
U_CPU	0
H_CPU	1



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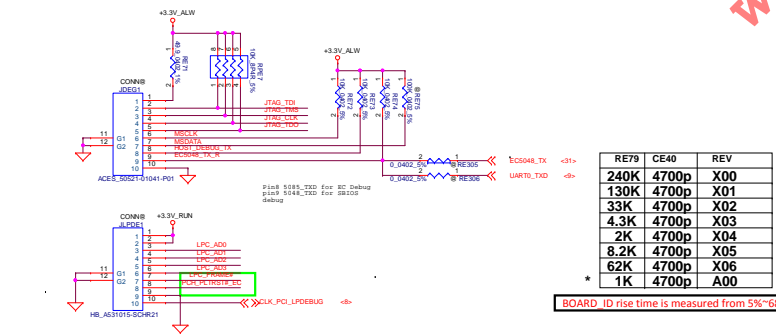
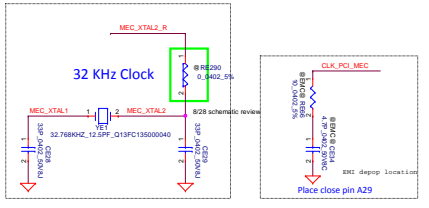
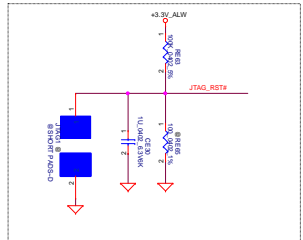
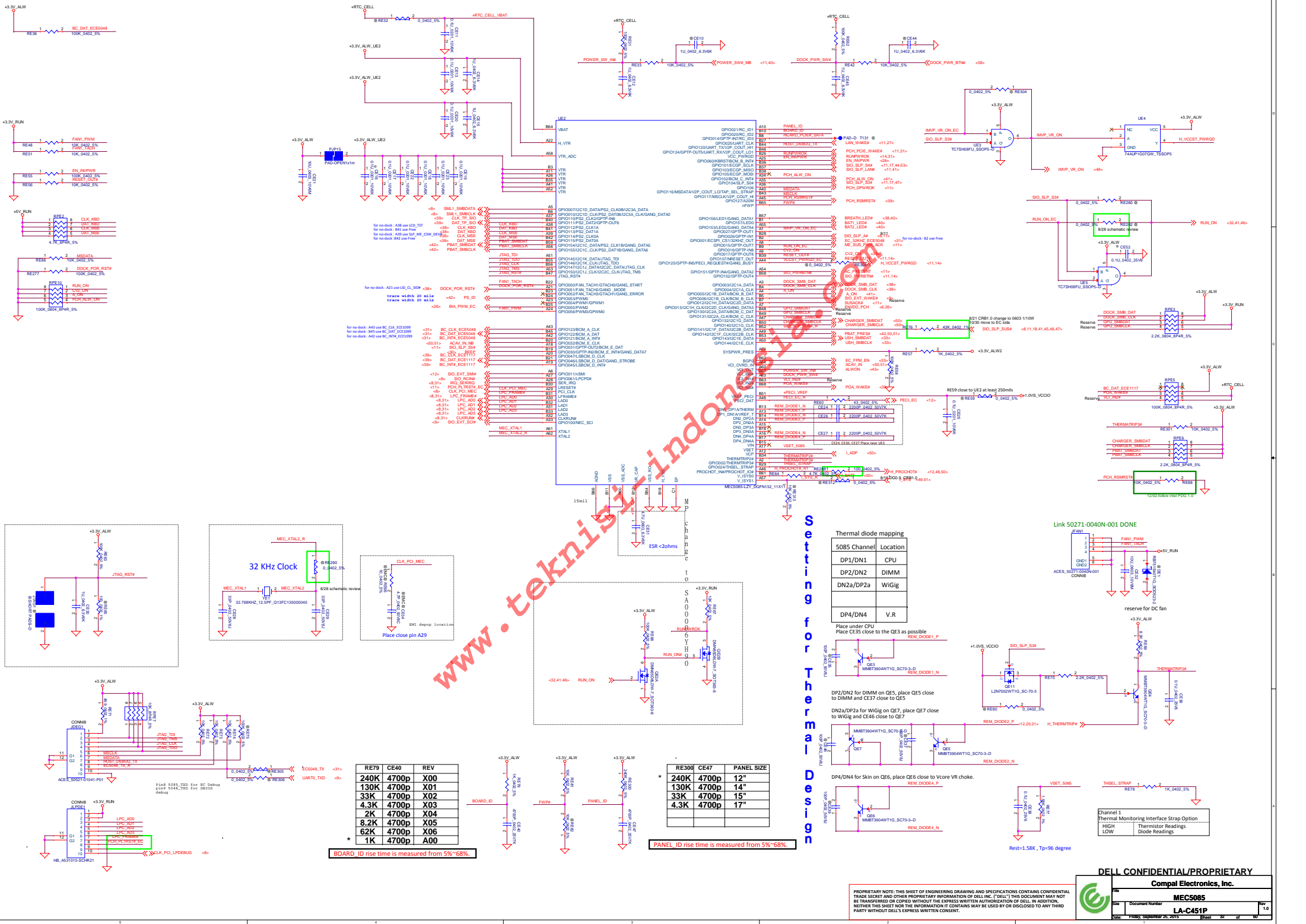
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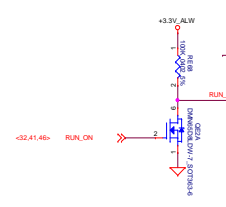
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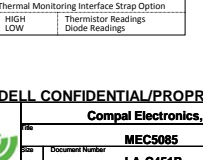
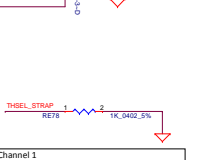
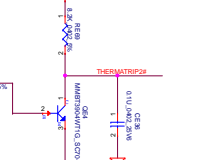
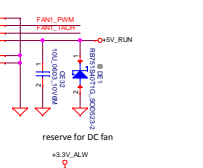
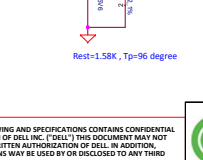
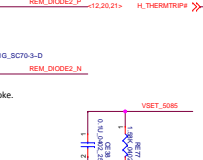
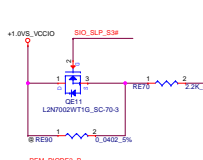
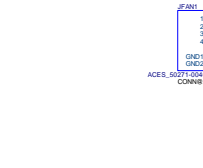
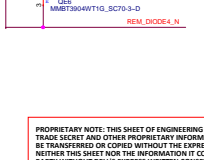
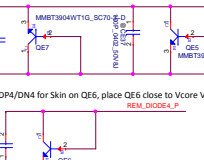
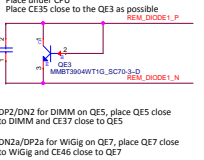
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	X04
8.2K	4700p	X05
62K	4700p	X06
1K	4700p	A00



RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

Setting for Thermal Design

Thermal diode mapping	
5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DN2a/DP2a	WiGig
DP4/DN4	V.R



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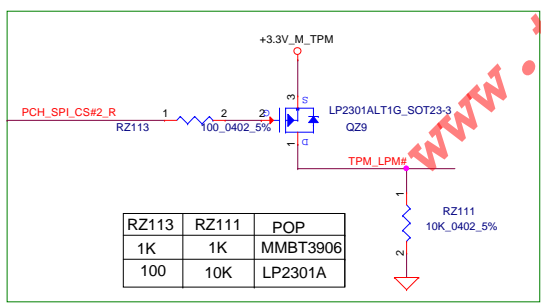
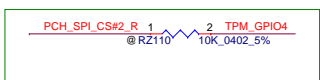
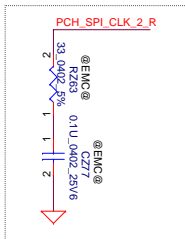
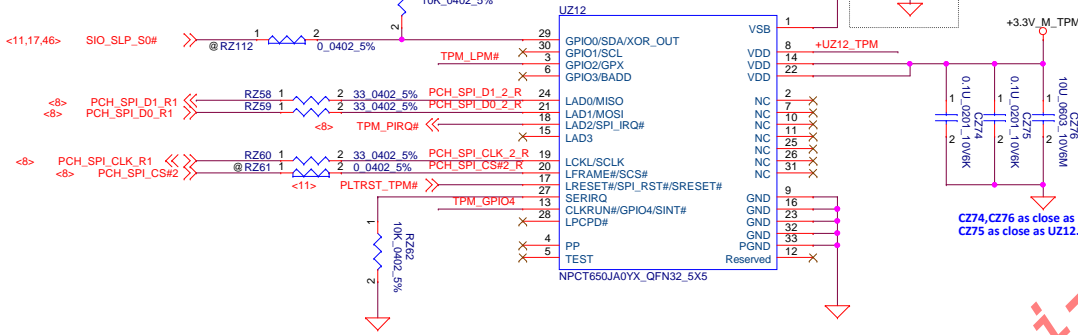
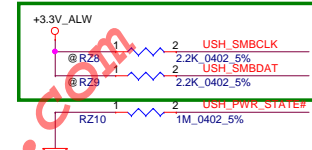
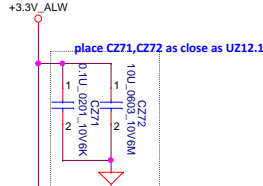
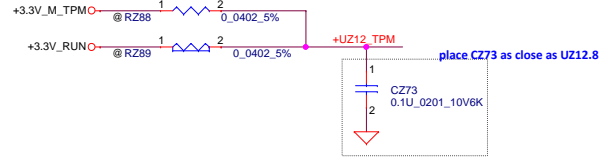
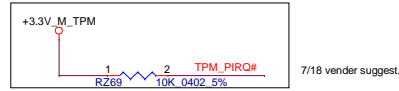
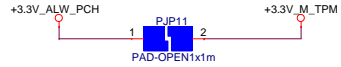
MEC5085

LA-C451P

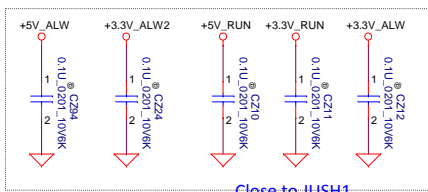
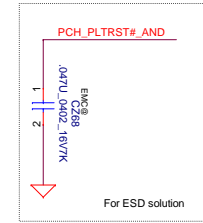
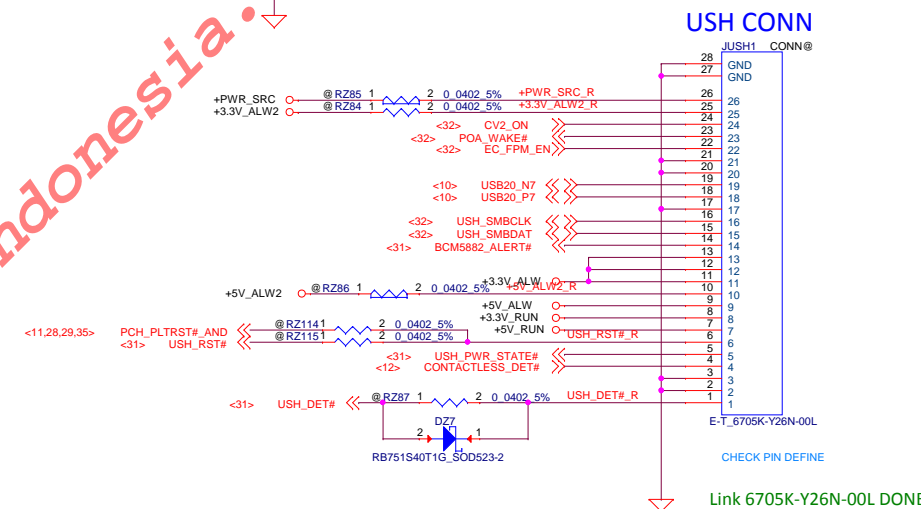
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power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)



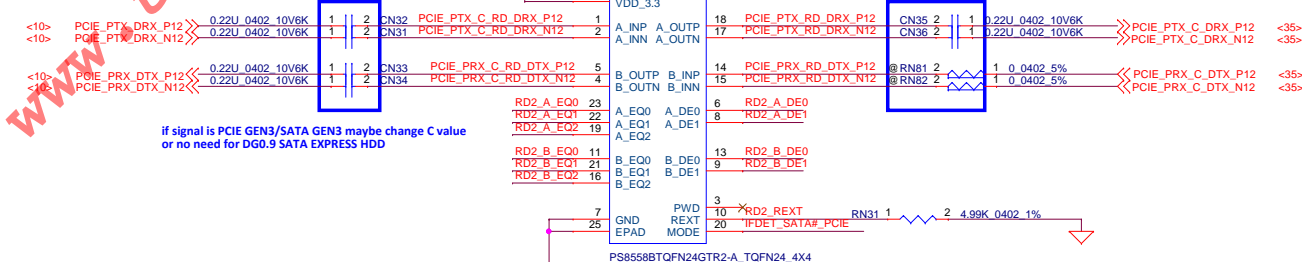
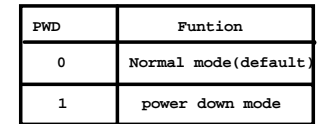
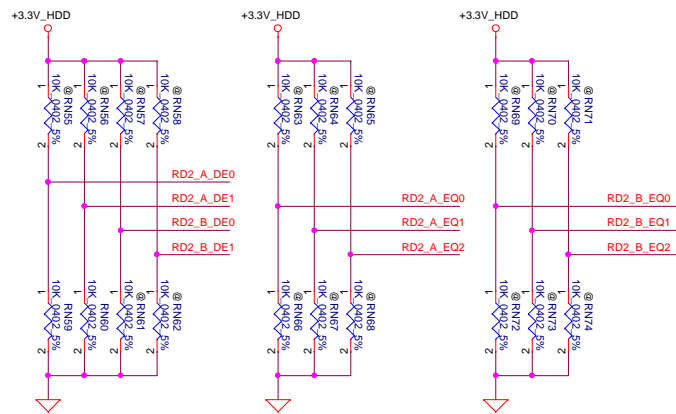
RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A



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Title		
USH & TPM		
Size	Document Number	Rev
		1.0
Date	Friday, September 25, 2015	Sheet 33 of 60

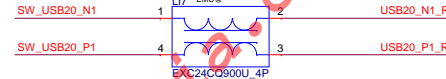
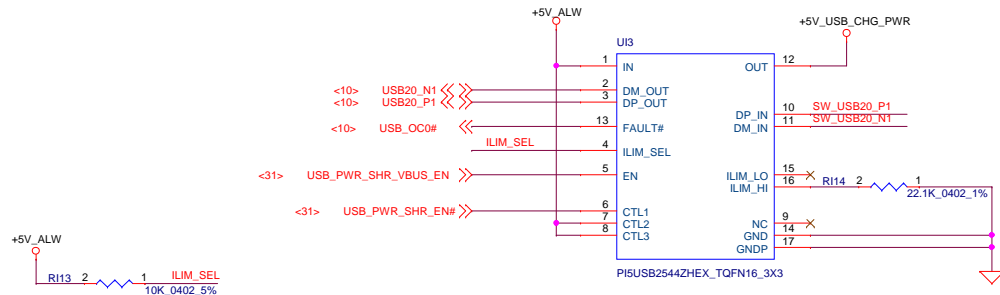
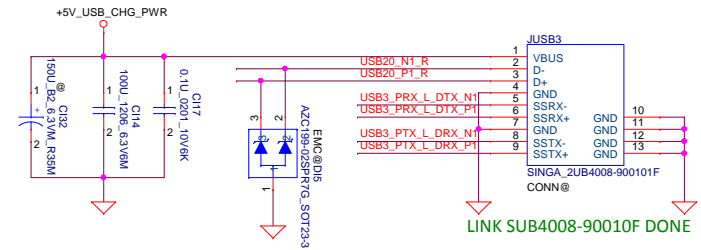
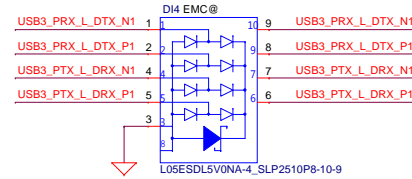
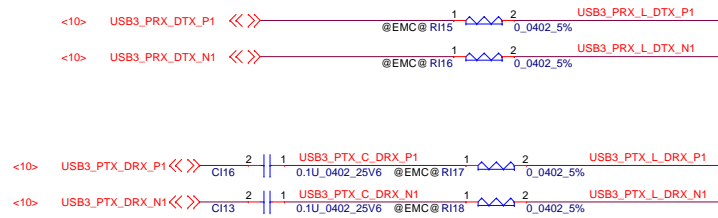
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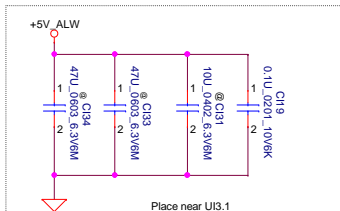
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

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Link Pericom PI5USB2544 Done
Change Selegro as main source



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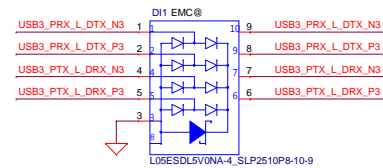
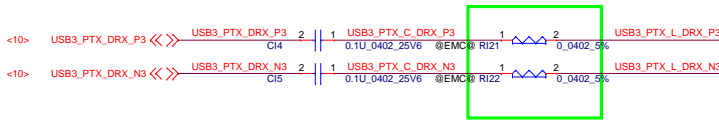
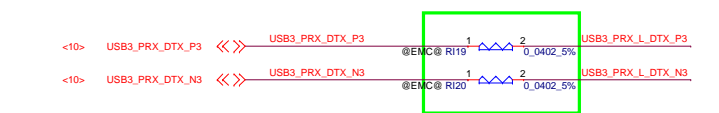
USB SW

LA-C451P

Rev 1.0

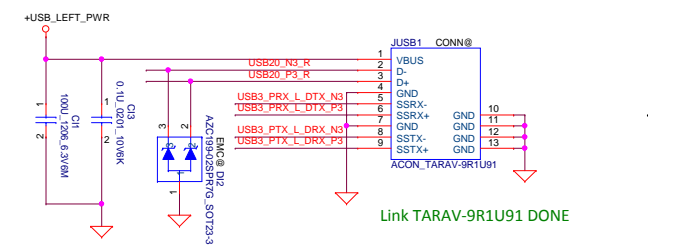
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Size	Document Number				
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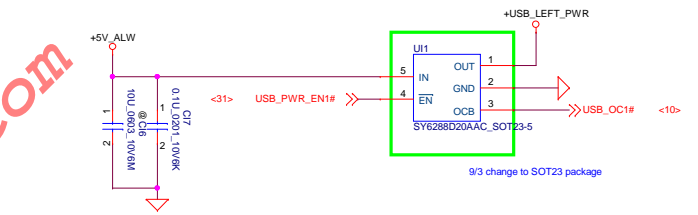


8/19 for layout routing change

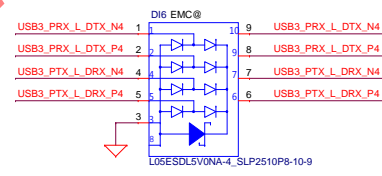
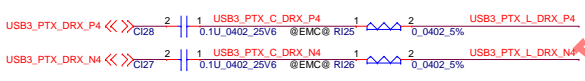
DFB request:
main: SM070003200 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (FANAAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



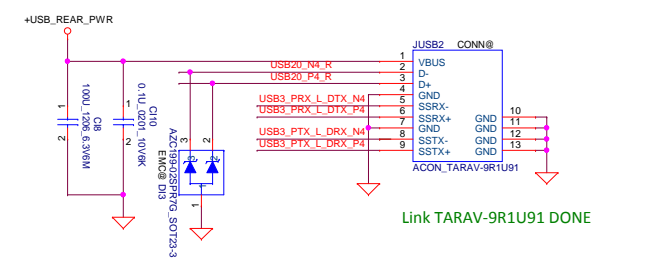
Link TARAV-9R1U91 DONE



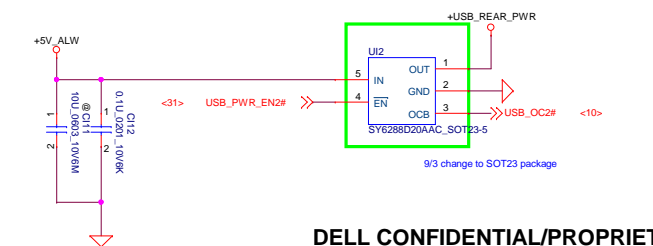
9/3 change to SOT23 package



8/19 for layout routing change



Link TARAV-9R1U91 DONE



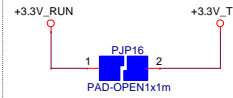
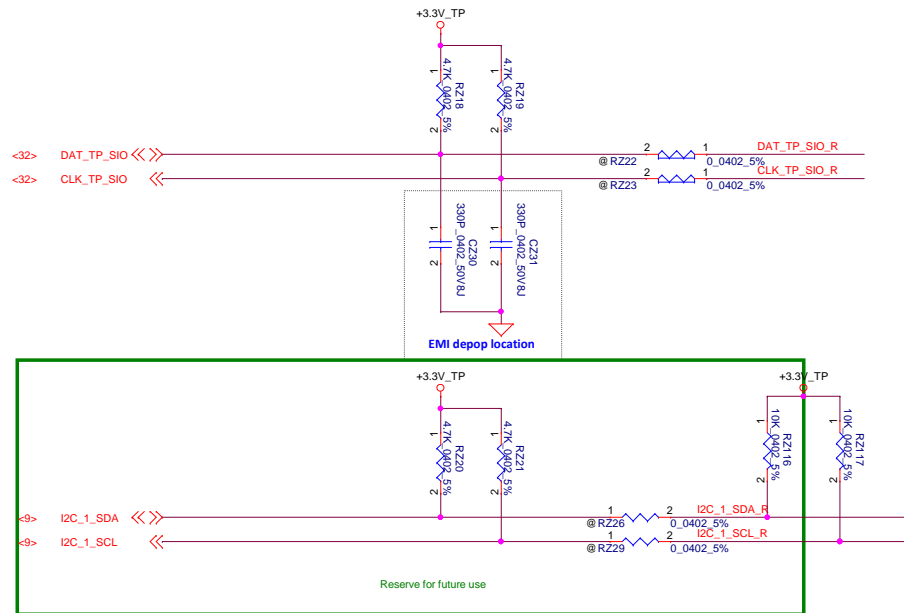
9/3 change to SOT23 package

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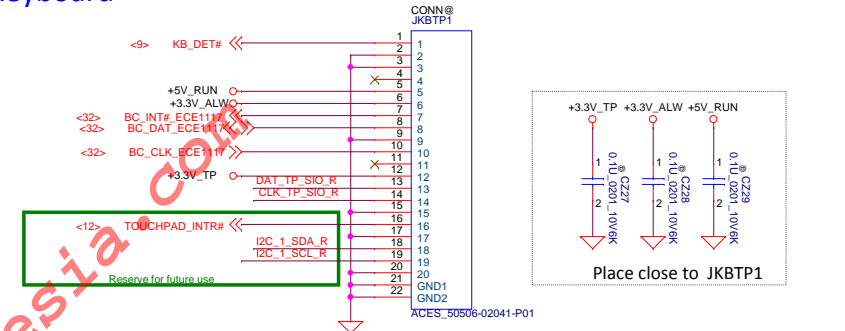
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Title	USB3.0		
Size	Document Number	LA-C451P	
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Touch Pad

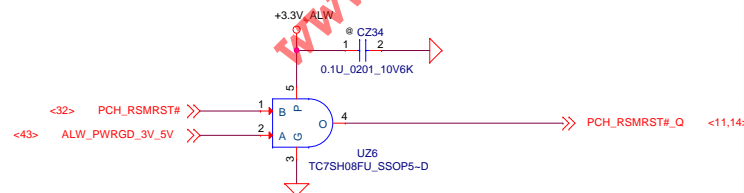


Keyboard



Link 50506-02041-P0 DONE

RSMRST circuit



@eDP Cable W CAM

Part Number	Description
DC02C007600	H-COHN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-COHN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-COHN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-COHN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-COHN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC301000100	CONN SET 13P DCJACK-MB 2DW1003-041110P

@BATT Cable

Part Number	Description
DC02001X800	H-COHN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JJ00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001D900	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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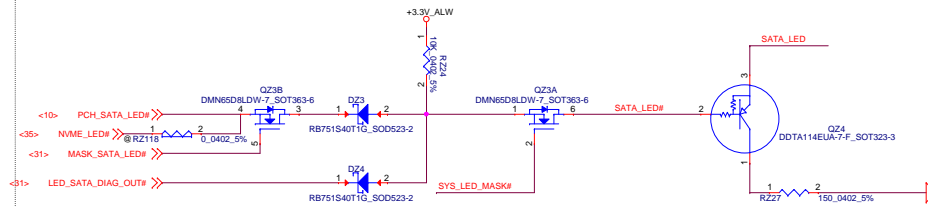
Keyboard

LA-C451P

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			1.0
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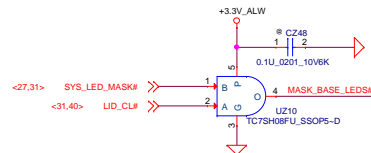
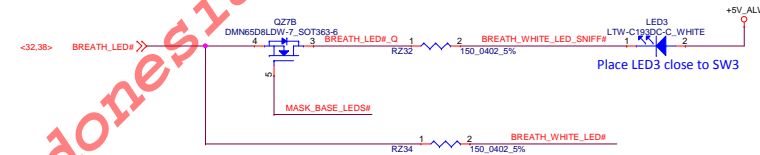
HDD LED solution for White LED



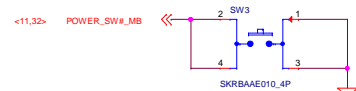
Battery LED



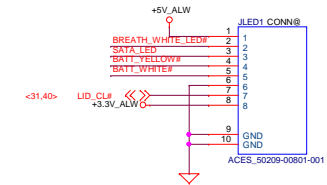
Breath LED



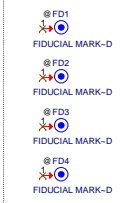
POWER & INSTANT ON SWITCH



LED board CONN

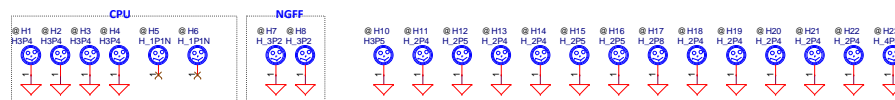


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



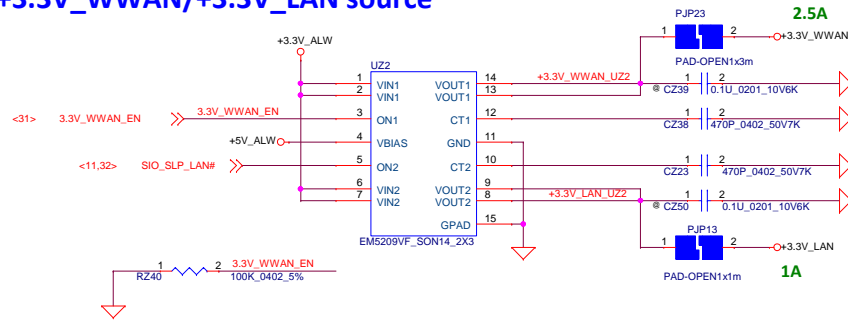
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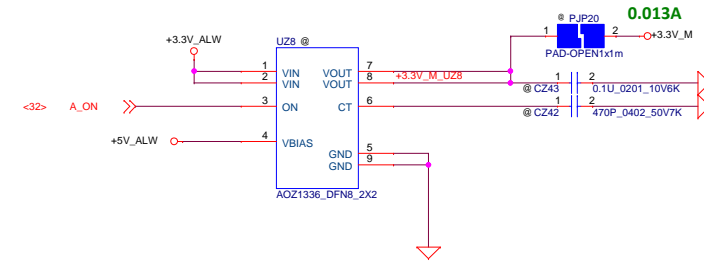
Compal Electronics, Inc.

File	Document Number	Rev
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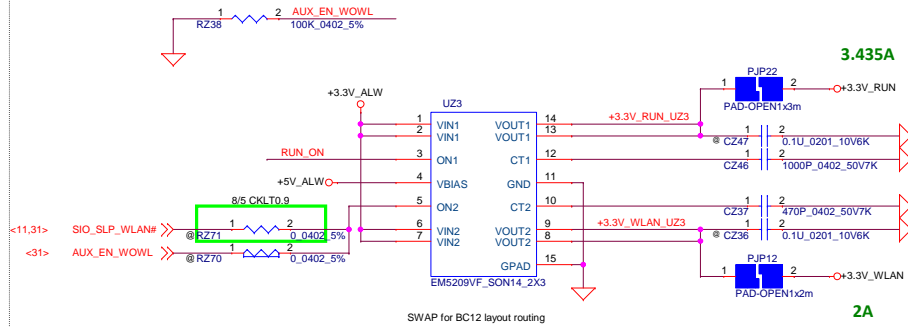
+3.3V_WWAN/+3.3V_LAN source



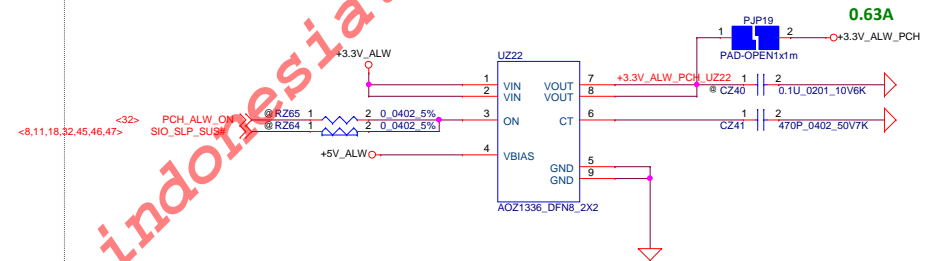
+3.3V_M source



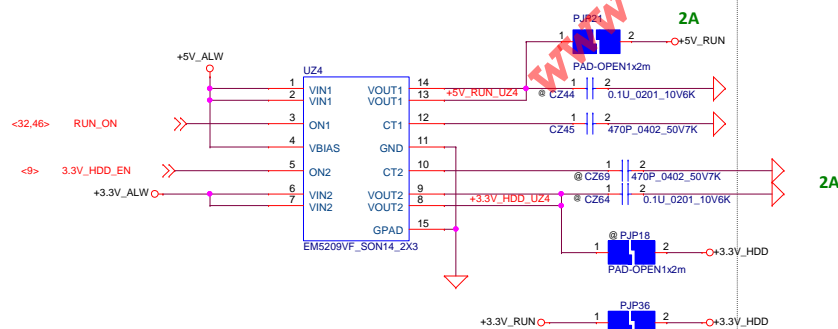
+3.3V_WLAN/+3.3V_RUN source



+3.3V_ALW_PCH source



+5V_RUN/+3.3V_HDD source



+3.3V_SUS source

Move to USH/B

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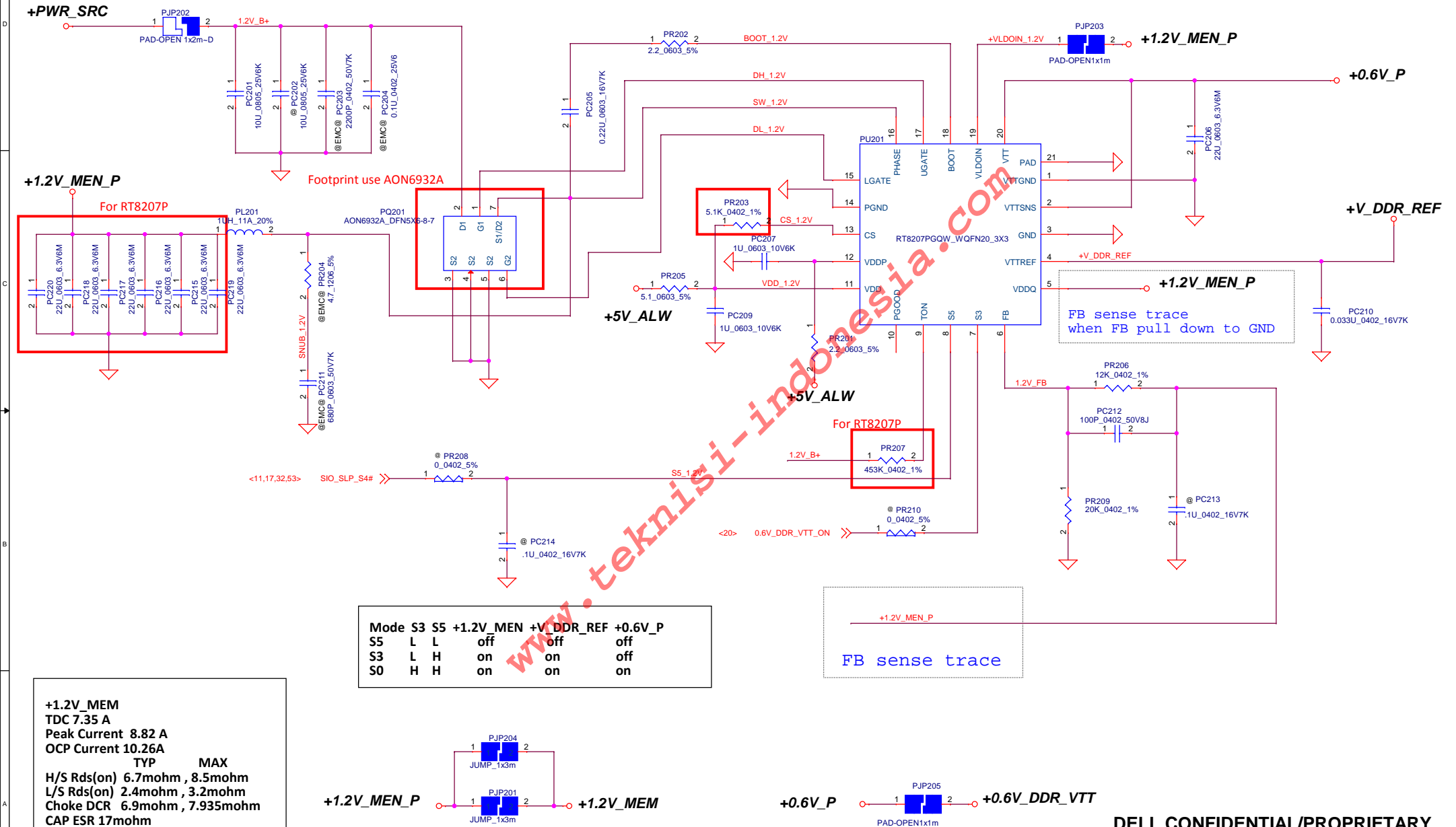
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Power control

LA-C451P

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0.6Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC



+1.2V_MEM
TDC 7.35 A
Peak Current 8.82 A
OCP Current 10.26A

	TYP	MAX
H/S Rds(on)	6.7mohm	8.5mohm
L/S Rds(on)	2.4mohm	3.2mohm
Choke DCR	6.9mohm	7.935mohm
CAP ESR	17mohm	

Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

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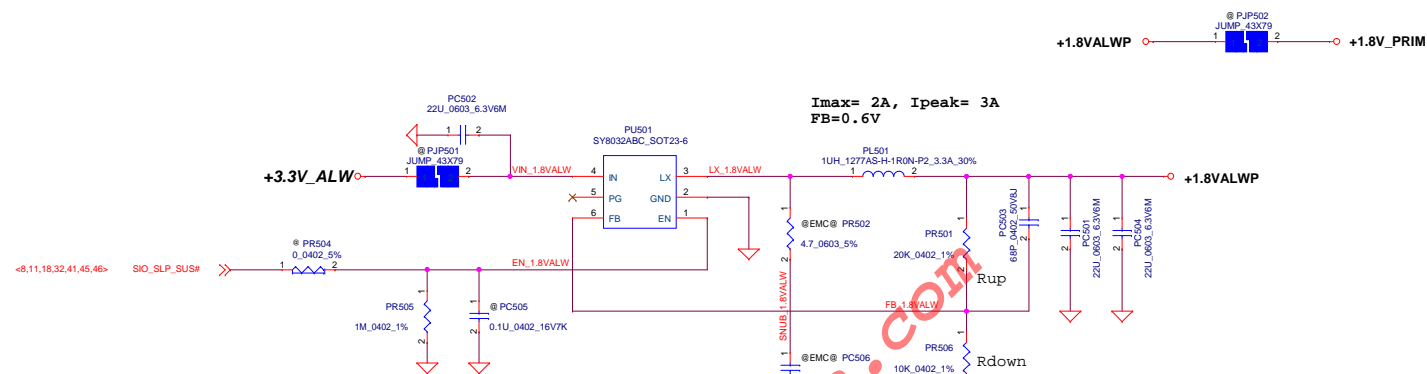
Compal Electronics, Inc.

+1.2V_MEN/+0.6V_DDR_VTT

LA-C451P

Date: Friday, September 25, 2015

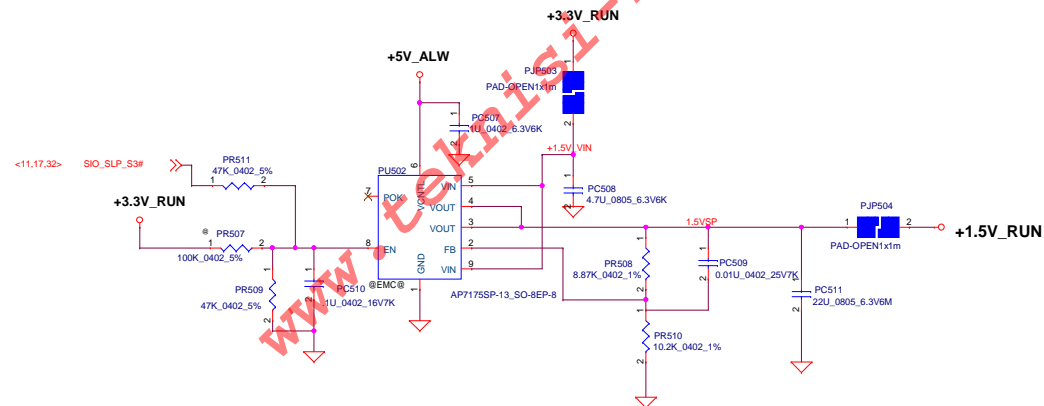
Sheet 44 of 60



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

+1.8V_PRIM
TDC 0.7 A
Peak Current 1.0 A
OCP Current 3.5A fix by IC



+1.5V_RUN
TDC 0.4 A
Peak Current 0.6 A
OCP Current 5.7 A fix by IC

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title	+1.8VALWP/+1.5V RUN	
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Local sense put on HW site

+1.0V_VCCST

VCC_SA
TDC 3.7A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm

VCCSA_B+ CPU_B+
PAD-OPENxtm

VCCSA_B+

+5V_RUN

+VCC_SA

+5V_ALW

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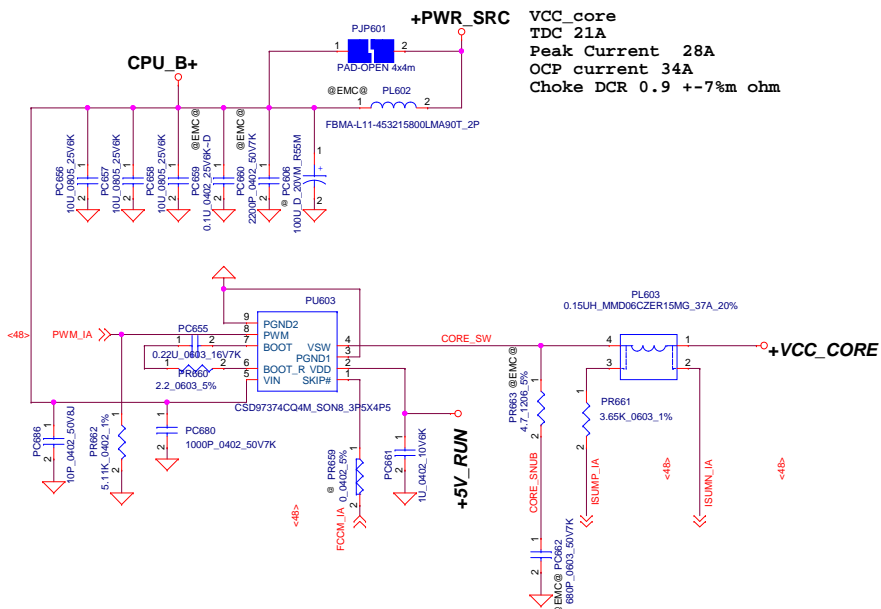
Compal Electronics, Inc.

PWR_VCORE_ISL95812 for QC

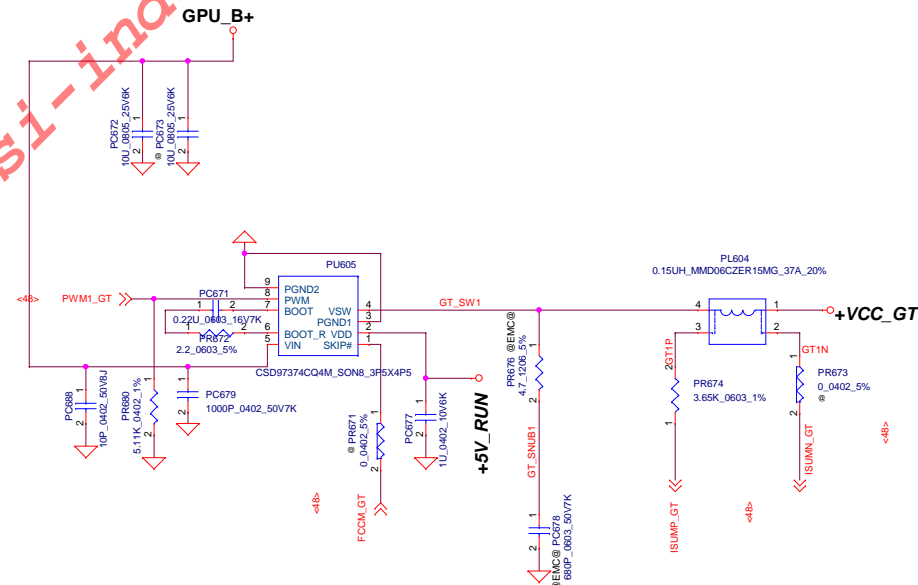
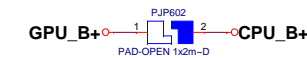
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VCC_GT
TDC 18A
Peak Current 31A
OCF current 37A
Choke DCR 0.9 +-7% ohm



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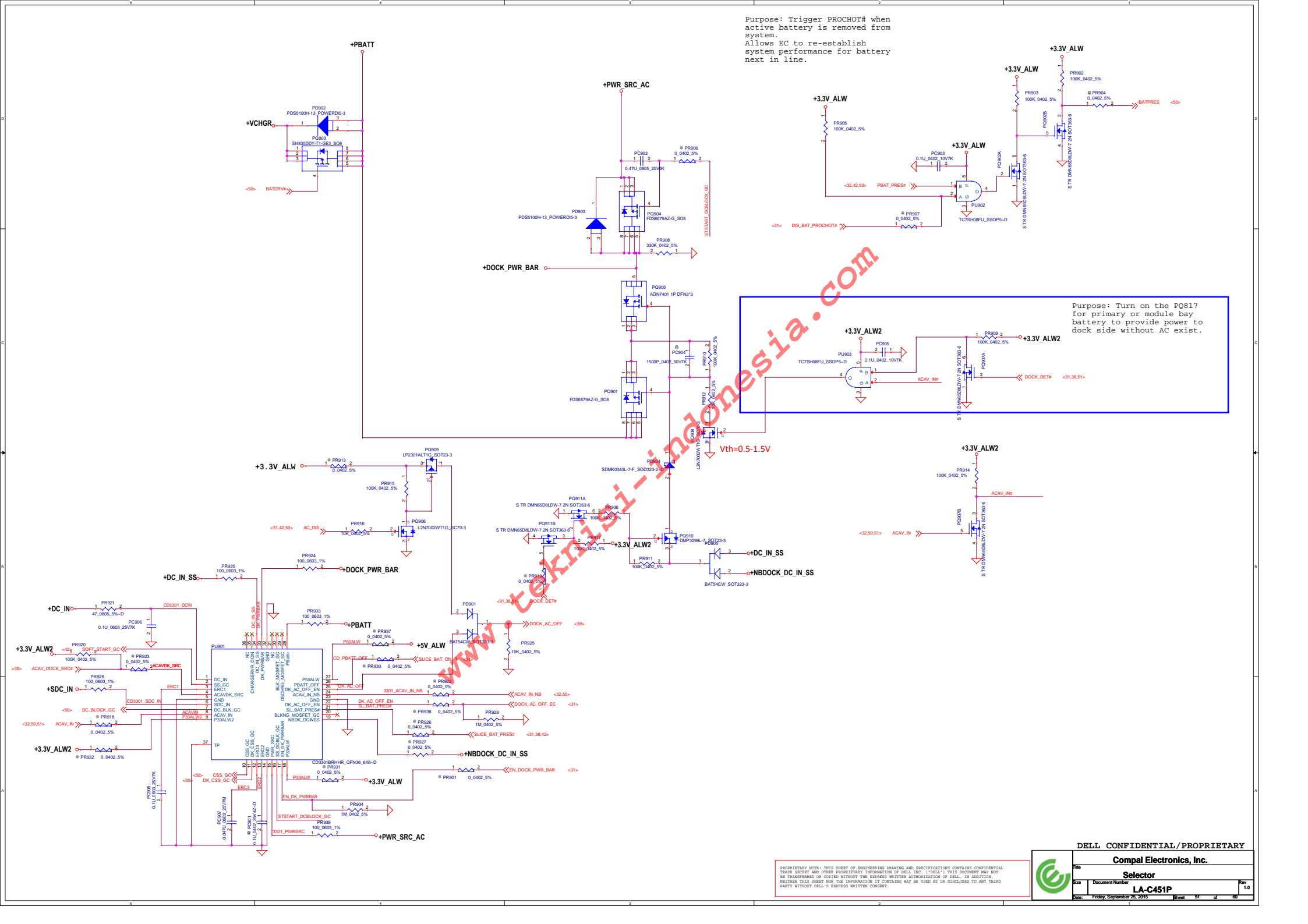
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PWR_VCORE_ISL95812 for QC			
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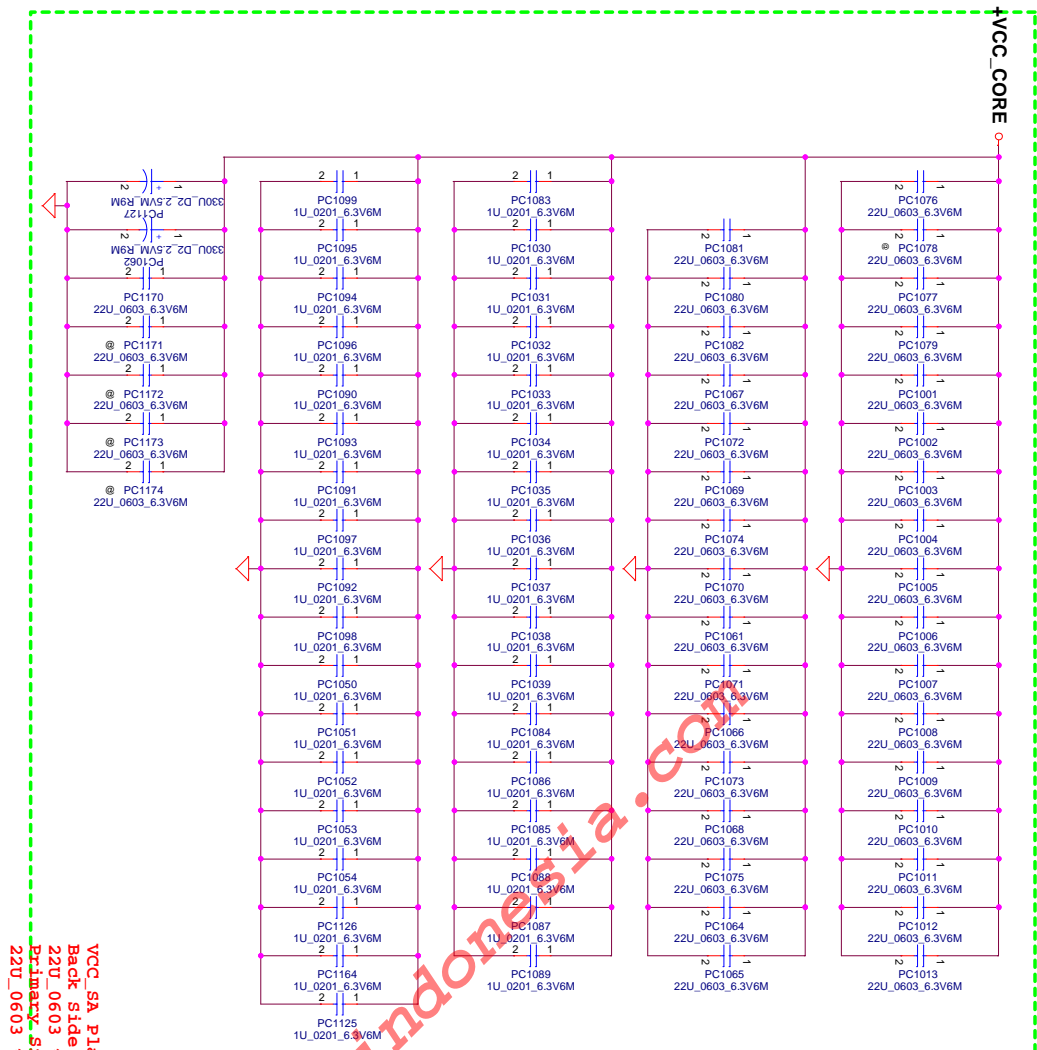
Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.

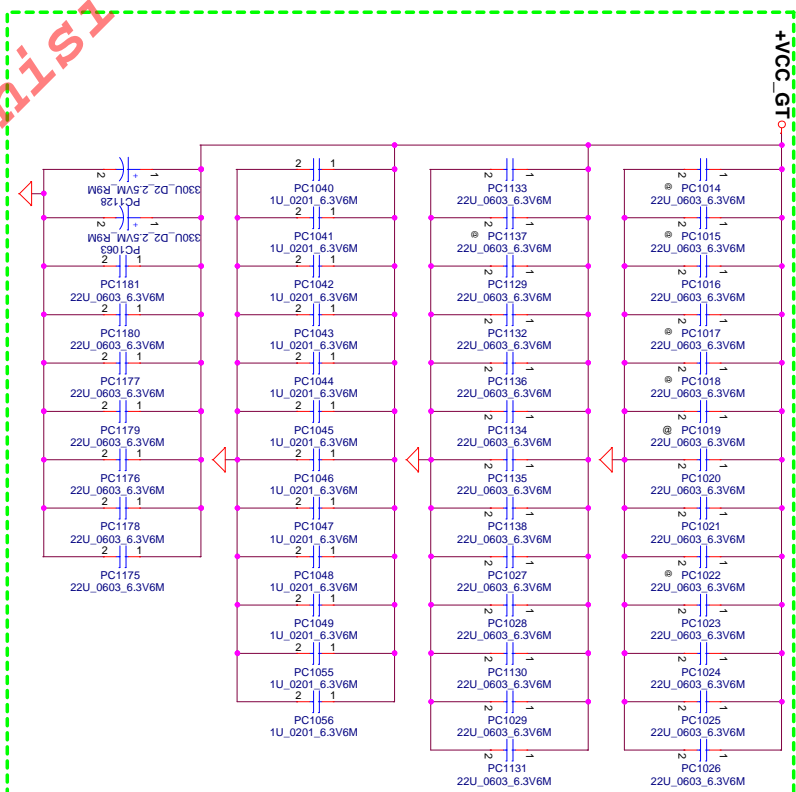


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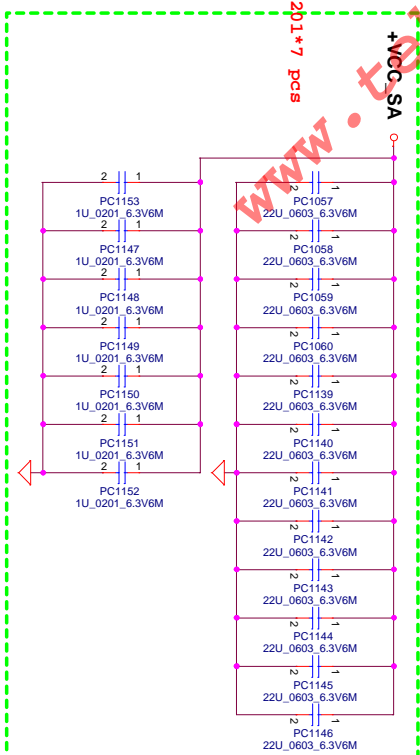
VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+330u_D2*2 pcs



VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +330u_D2*2 pcs



VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs



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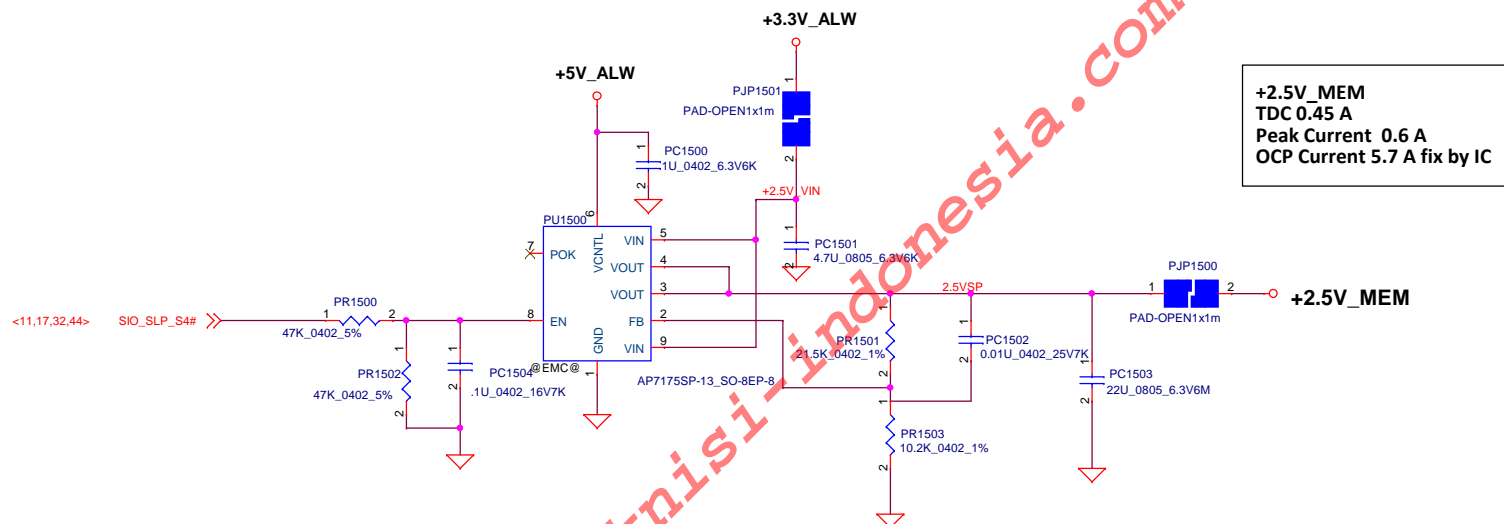
PROCESSOR DECOUPLING

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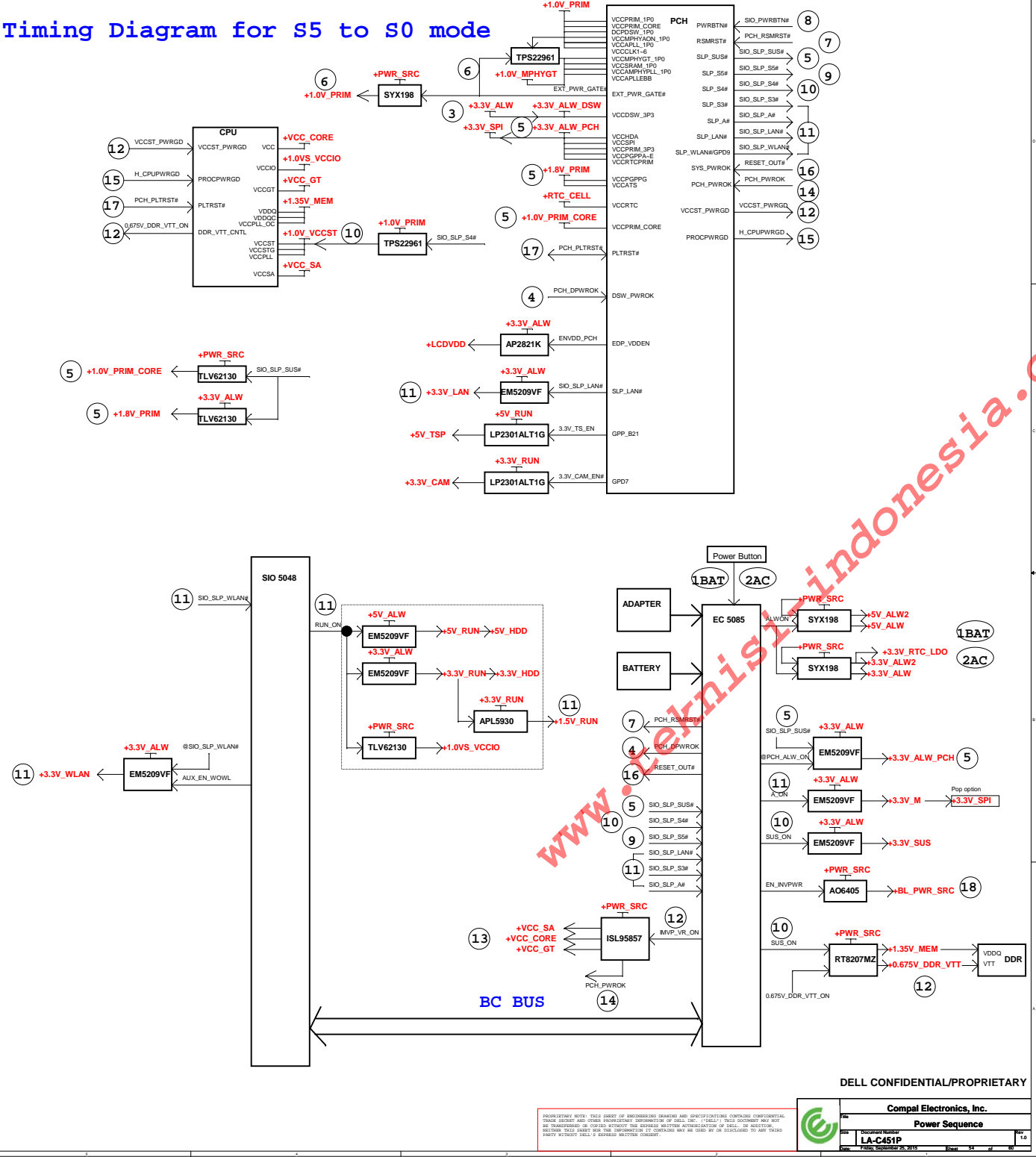


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Timing Diagram for S5 to S0 mode



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Version Change List (P. I. R. List)


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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7,17,20,21	HW	2014/11/17	COMPAL	Change DDR3L to DDR4 schematic	1. JDIMM1&JDIMM2 change from DDR3L to DDR4 connector 2. change +1.35V_MEM to +1.2V_MEM 3. change +0.675V_DDR_VTT to +0.6V_DDR_VTT 4. add +2.5V_MEM	0.2(X01)
2	10,32,34	HW	2014/11/17	COMPAL	EC MCARD_PCIE#_SATA pin is for WWAN slot, not KEY M SSD slot	1. QN2.1&UC1.H2&RC174.1 change from MCARD_PCIE#_SATA to IFDET_SATA_PCIE#	0.2(X01)
3	9	HW	2014/11/17	COMPAL	For reduce power comsupition	RC287 change from 10k to 100k ohm	0.2(X01)
4	34	HW	2014/11/19	COMPAL	For key M slot PCIE/SATA Detect	Delete QN2/RN48/RN24, IFDET_SATA#_PCIE connect to PCH directly (BIOS need setup SATA=0:PCIE=1 by PSCPSP_Px_STRP bit=1)	0.2(X01)
5	8,11,27	HW	2014/11/20	COMPAL	Follow Intel LAN Review result	1.RC19&RC20 PH change from +3.3V_ALW_PCH to +3.3V_LAN 2.CL7 change from 1uF to 0.1uF 3.CL4 add @ 4.CL16&CL17&CL20&CL21 change from 0.47uF to 0.1uF 5.RC70 PH change from +3.3V_ALW_DSW to +3.3V_LAN	0.2(X01)
6	36	HW	2014/11/20	COMPAL	Follow Pericom Review result	Reserve CI31	0.2(X01)
7	31,32	HW	2014/11/21	COMPAL	Follow Gen7 GPIO Master_1122	1.AC_DIS change from UE2.A10 to UE1.A50 2.Add PANEL_ID at UE2.A10 and RE300&CE47 3.Delete RE291 & RE281,and change SUS_ON to CV2_ON	0.2(X01)
8	27	HW	2014/11/25	COMPAL	Follow Intel LAN Review result	1.CL22 change from 150P to 1500P 2KV(SE00000WQ00)	0.2(X01)
9	30	HW	2014/11/25	COMPAL	Follow Intel WOV(Wake on Voice) suggest	1.Delete RA15/RA41/RA42	0.2(X01)
10	34	HW	2014/11/25	COMPAL	Remove co-lay schematic with PS8558B	1.Delete CN43~CN46,RN85,RN86,UN89~RN98	0.2(X01)
11	32	HW	2014/11/25	COMPAL	For separate +1.2V_MEM&+3.3V_CV2 enable pin	1.Delete RE291&RE281	0.2(X01)
12	11,12,14	HW	2014/11/25	COMPAL	For ESD request	1.Add CC300 100P at H_VCCST_PWRGD 2.Add CC301 100P at H_CPUPWRGD 3.Reserve CC302 0.1u at SYS_RESET# 4.Reserve CC303 0.1u at PCH_JTAG_TDO 5.Reserve CC304 0.1u at PCH_JTAG_TDI 6.Reserve CC305 0.1u at XDP_JTAGX 7.Reserve CC306 0.1u at TDD_XDP 8.Reserve CC307 0.1u at H_VCCST_PWRGD_XDP 9.Reserve CC308 0.1u at CPU_XDP_TRST#	0.2(X01)
13	20,21	HW	2014/11/25	COMPAL	Follow Intel DDR4 Review result	1.CD24~CD27,CD57~CD60 change from 0.1uF to 1uF 2.CD29,CD62 add @ 3.+2.5V_MEM add CD70,CD71,CD74,CD75(1UF) & CD72,CD73,CD76,CD77(10UF) 3.+1.2V_MEM add CD78~CD85,CD102~CD109(1UF)&CD86~CD101(10UF)	0.2(X01)
14	38	HW	2014/12/01	COMPAL	For sync up with PARK CITY DSC port mapping	Swap USB2.0 port5 & port6 at JDOCK1	0.2(X01)
15	32	HW	2014/12/01	COMPAL	Board ID for X01	RE79 change from 240k ohm to 130k ohm	0.2(X01)

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16	31,32	HW	2014/12/01	COMPAL	Follow Gen7 GPIO Master_1127	1.Delete RE294/RE295/RE296/RE297 2.5085 GPIO116 change from PCH_PCIE_WAKE# to MSDATA 3.5085 GPIO124 change from ME_FWP_EC to PCH_PCIE_WAKE# 4.5048 GPIOJ1 add ME_FWP_EC 5.5085 GPIO117 change from USB_PWR_SHR_EN# to MSCLK 6.5048 GPIOK0 add USB_PWR_SHR_EN#	0.2(X01)
17	32	HW	2014/12/02	COMPAL	Follow INTEL PDG 1.0	Charger SMBUS PU resistor change from 10k to 2.2k	0.2(X01)
18	32	HW	2014/12/02	COMPAL	Follow INTEL PDG 1.0	RE88 change from 47k to 10k	0.2(X01)
19	39	HW	2014/12/05	COMPAL	Follow Dell ARD Rev1.3	1.Reserve RZ26/RZ29 for I2C_1_SDA/I2C_1_SCL 2.Add RZ22/RZ23 for DAT_TP_SIO/CLK_TP_SIO	0.2(X01)
20	13	HW	2014/12/05	COMPAL	Follow 546765_546765_2014WW48_Skylake_MOW_Rev_1_0	RC120 add @	0.2(X01)
21	32	HW	2014/12/09	COMPAL	For Port Mapping update	1.For USB2, Camera change from port 10 to port 2 WWAN change form port 2 to port 10 2.For USB3, EDOCK change from port 5 to port 2 WWAN change from port 2 to port 5 3.For SATA, EDOCK change from SATA1B to SATA1A 4.For PCIE/SATA, M2 SSD PCIE lane 0 change from port 7 to port 12, M2 SSD PCIE lane 1 change from port 8 to port 11	0.2(X01)
22	11	HW	2014/12/27	COMPAL	For PLTRST glitch issue	1.UC7.5 change from +3.3V_RUN to +3.3V_ALW_PCH 2.Pop RC325,depop RC60	0.3(X02)
23	11	HW	2014/12/29	COMPAL	For DIMM Select Issue	Pop RD63 ;Depop RD67	0.3(X02)
24	22	HW	2014/12/29	COMPAL	For HDMI EMI solution	1.add RV647~RV658	0.3(X02)
25	32	HW	2014/12/30	COMPAL	For Layou routing	1.Swap LV3,LV6,LV9,LV12	0.3(X02)
26	32	HW	2014/12/29	COMPAL	For Power down sequence	1.add QE8,UE4,RE304,RE305	0.3(X02)
27	8	HW	2014/12/31	COMPAL	For Support DCI	1.Reserve RC326,QC3, Add RC327	0.3(X02)
28	13	HW	2014/12/31	COMPAL	Follow 546765_546765_2014WW52_Skylake_MOW_Rev_1_0	1.Reserve CC222 and RC313	0.3(X02)
29	33	HW	2015/02/06	COMPAL	For TPM issue	1.UZ12.29 reserve RZ90(10K) PU to +3.3V_RUN 2.UZ12.3 add TPM_LPM# signal & QZ9,RZ111 3.UZ12.13 add TPM_GPIO4 signal &Reserve RZ110 4.Add RZ88(+3.3V_M_TPM), Reserve RZ89(+3.3V_RUN)	0.4(X03)
30	12	HW	2015/02/06	COMPAL	For support DCI	1.add RC328 between CPU_XDP_TCLK & XDP_JTAG 2.add RC329,Reserve RC340 3.Pop QC3,depop RC327	0.4(X03)
31	10	HW	2015/02/06	COMPAL	For fix DCI warmboot hang up issue	1.USB2_ID add RC337(10K) to GND 2.USB2_VBUSSENSE add RC338(10K) to GND	0.4(X03)

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32	32	HW	2015/02/06	COMPAL	For Power down sequence	Depop RE304,RE305,pop UE3	0.4(X03)
33	11	HW	2015/02/06	COMPAL	For auto power on issue	Depop RC70, depop RC323	0.4(X03)
34	26	HW	2015/02/06	COMPAL	BOM changed,follow PC	UV24 from SA00006EE00(AP2821KTR-G1) to SA00006Y800(G524B1T114)	0.4(X03)
35	8	HW	2015/03/02	COMPAL	Intel MOW_2015WW06:Intel recommendation for DCI tool consulting,	RC317 change from 4.7k to 150k ohm	0.4(X03)
36	32	HW	2015/03/02	COMPAL	For X03 Board ID	RE79 change from 130k to 4.3k	0.4(X03)
37	8	HW	2015/03/02	COMPAL	Intel MOW_2015WW06:Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update	de-pop RC30, RC316	0.4(X03)
38	33	HW	2015/03/02	COMPAL	for allow further reducing power in TPM 2.0 F/W,when system is in S3/4/5 and main power is off.	Pop RZ90	0.4(X03)
39	34	HW	2015/03/02	COMPAL	Follow SATA EA result	pop RN59 &RN60	0.4(X03)
40	20,21	HW	2015/03/02	COMPAL	Intel MOW_2015WW02	Depop CD6,CD35	0.4(X03)
41	35,12	HW	2015/03/02	COMPAL	For ESD request	1.H_THERMTRIP# reserve CC309 0.1uF to GND 2.H_PROCHOT# reserve CC310 0.1uF to GND	0.4(X03)
42	12	HW	2015/03/02	COMPAL	For RF request	1.CC3~CC6 change from 12pF to 27pF & pop 2.HDA_SDOOUT add CC311 15pF to GND	0.4(X03)
43	26	HW	2015/03/02	COMPAL	Reserve for IR camera	Reserve JIR1	0.4(X03)
44	33	HW	2015/03/04	COMPAL	For TPM vender review result	UZ12.29 reserve RZ112 to SIO_SLP_S0#	0.4(X03)
45	9	HW	2015/03/04	COMPAL	For support DDR3L & DDR4	UC1.P2 add DIMM_TYPE signal;Low(RC342)=DDR4,High(RC341)=DDR3L	0.4(X03)
46	36	HW	2015/03/04	COMPAL	For USB charger issue	UI3 change from SA00007TJ00(Pericom) to SA00008DH00(Selegro)	0.4(X03)
47	11,32	HW	2015/03/06	COMPAL	For Crystal EA	CC21/CC22 change to 15pF CE28/CE29 change to 33pF	0.4(X03)
48	8	HW	2015/03/06	COMPAL	Follow INTEL CRB	RC23 change from 8.2k to 2.2k	0.4(X03)
49	33	HW	2015/04/17	NUVOTON	For support modern standby	1. Pop RZ112(0 ohm) & Depop RZ90(10k ohm)	0.5(X04)
50	33	HW	2015/04/17	NUVOTON	For TPM schematic review	1. Pop RZ89(0 ohm) & Depop RZ88(0 ohm) 2. Add RZ113(100 ohm)	0.5(X04)

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51	9,11	HW	2015/04/17	COMPAL	For backdrive issue	1. DIMM_TYPE PU change from +3.3V_ALW to +3.3V_ALW_PCH 2. VRALERT# PU change from +3.3V_ALW to +3.3V_ALW_PCH	0.5(X04)
52	9,26	HW	2015/04/17	COMPAL	For IR camera design	1. add IR_CAM_DET# connect between GPP_A23(UC1.AW7) & JIR1.6 2. JIR1.3 change from +PWR_SRC to NC	0.5(X04)
53	31,33	HW	2015/04/17	Broadcom	Reserve for USH RESET	UE1.A62 add USH_RST#, and reserve RZ114&RZ115 on JUSH1.21	0.5(X04)
54	12	HW	2015/04/17	COMPAL	For wake up system when non-deep S3	SIO_EXT_SMI# PU change from +3.3V_RUN to +3.3V_ALW_PCH	0.5(X04)
55	10	HW	2015/04/17	INTEL	For DCI function	RC337 change from 1k to 0 ohm	0.5(X04)
56	29	HW	2015/04/17	COMPAL	SIM detect	Add RI31 connecting with JSIM1.9 and NGFF2.58	0.5(X04)
57	29	HW	2015/04/17	COMPAL	ME request	JSIM1 change from JAE_SF51S006V4B to T-SOL_5-991503004000-6	0.5(X04)
58	41	HW	2015/04/17	COMPAL	For +3.3V_HDD power solution	Depop PJP18,CZ69; Pop PJP36	0.5(X04)
59	39	HW	2015/04/17	COMPAL	For new U1 TP module	Add RZ116 and RZ117 PU on I2C_1_SDA_R/I2C_1_SCL_R	0.5(X04)
60	8	HW	2015/04/21	COMPAL	For LAN backdrive	1. Add RC347 and RC348 PU to +3.3V_ALW_PCH 2. Depop RC19,RC20	0.5(X04)
61	32	HW	2015/04/21	COMPAL	For Board ID	RE79 change from 4.3k to 2k	0.5(X04)
62	14	HW	2015/04/23	COMPAL	For DCI function	UC8 & CC30 remove CXDP@	0.5(X04)
63	22	HW	2015/04/24	COMPAL	Base on HDMI EE/EMI measure result	Pop LV3/LV6/LV9/LV12 Depop RV647~RV658	0.5(X04)
64	40	HW	2015/04/29	COMPAL	ME request	Add H28 H_2P3	0.5(X04)
65	40	HW	2015/04/29	COMPAL	For JAE JSIM1 boss hole	Add H29 H_0P7N & H30 H_0P9N	0.5(X04)
66	36	HW	2015/05/04	COMPAL	For 儲存巴士 shut down issue	Add CZ32 (150U_B2_6.3VM_R35M)	0.5(X04)
67	39	HW	2015/05/06	COMPAL	For TP sometimes can't work in BIOS or OS	Pop CZ30/CZ31 330pF	0.5(X04)
68	29,40	HW	2015/05/12	COMPAL	For NVME SSD LED issue	JNGFF3.10 add NVME_LED#, thought RZ118(0 ohm) connect to PCH_SATA_LED#	0.5(X04)
69	36	HW	2015/05/12	COMPAL	For USB charger issue	UI3 main source change from SA00008DH00(Selegro) to SA00007TJ00(Pericom)	0.5(X04)
70	40	HW	2015/05/12	COMPAL	Base on LED EA result	RZ25/RZ27/RZ34 change from 220 to 150 ohm	0.5(X04)
71	18	HW	2015/05/28	INTEL	For RF 5.76GHz noise issue	1. add RC349,CC313,CC314 2. change 0603 to 0402	0.5(X04)
72	27	HW	2015/06/02	COMPAL	For LAN EA result	Change LL2~LL9(12nH) to RL71~RL78(2.2ohm)	0.5(X04)
73	22	HW	2015/06/02	COMPAL	For HDMI EA result	1.RV647/RV649/RV650/RV652/RV653/RV655/RV656/RV658 change from 8.2ohm to 5.6 ohm 2.RV648/RV651/RV653/RV657 change from 150 ohm to 200 ohm 3.Depop LV3/LV6/LV9/LV12;Pop RV647~RV658	0.5(X04)

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74	25	HW	2015/06/03	COMPAL	For DP hub display flicker issue	1.Add UV29,CV617,CV618,CV619,PJP37,RV659,RV650,RV661 2.Depop UV28,PJP33	0.5(X04)
75	9	HW	2015/06/04	COMPAL	Sink up with Park City	Reserve RC330,RC331	0.5(X04)
76	33	HW	2015/07/13	DELL	IC change from TPM2.0 to TPM1.2	UZ12 change from SA000082D00(TPM2.0) to SA000082D20(TPM1.2)	0.6(X05)
77	33	HW	2015/07/13	NUVOTON	For TPM Deep S3 issue	UZ12.1 change from +3.3V_ALW_PCH to +3.3V_ALW	0.6(X05)
78	32	HW	2015/07/13	COMPAL	For Global Reset issue	1.Add UE5,QE11 & Reserve CE52,RE90 2.RE292 footprint change from 0ohm-short to 0 ohm(@)	0.6(X05)
79	32	HW	2015/07/13	COMPAL	For Board ID	RE79 change from 2k to 8.2k	0.6(X05)
80	18	HW	2015/07/17	COMPAL	For RF request	1.Change RC349/RC172(0 ohm) to LC1/LC2(BLM15HG601SN1D) 2.Pop CC313/CC314	0.6(X05)
81	36	HW	2015/07/17	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	0.6(X05)
82	17	HW	2015/08/17	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control to +VCCPLL_OC power rail	0.7(X06)
83	17	HW	2015/08/17	COMPAL	Follow Park City for DC mode CPU trubo issue	Reserved RE313 pull down path on I_SYS	0.7(X06)
84	17	HW	2015/08/17	COMPAL	Change design soluiton for prevent thermal too high	UV29 change from APL5930QBI-TRG_TDFN10_3X3 to G9661-25ADJRE1U_TDFN10_3X3 & VIN change from +3.3V_RUN to +1.8V_PRIM	0.7(X06)
85	32	HW	2015/08/19	COMPAL	For Board ID	RE79 change from 8.2k to 62k	0.7(X06)
86	36	HW	2015/08/27	COMPAL	For 儲存巴士 & Dell USB HDD issue at Low battery on 3 cell battery	1.Pop CI14; depop CI32 2,UI3 change from SA00007TJ00 to SA000097E00 3.Reserve CI33,CI34	0.7(X06)
87	9	HW	2015/09/09	COMPAL	Add GPIO for China TPM & TPM option	add TPM_TYPE signal &RC349	1.0(A00)
88	8	HW	2015/09/09	COMPAL	For TP issue	Depop CC4	1.0(A00)
89	32	HW	2015/09/09	COMPAL	For Board ID	RE79 change from 62k to 1k	1.0(A00)
90	12,28,32,27	HW	2015/09/09	COMPAL	For MP	1.Depop SW1, RC221 change to 0 ohm short pad 2.UR2 change from SA000089Q00 to SA000089Q10 3.U2 change from SA00006YH30 to SA00006YH90 4.UL1 change from SA000081G0L to SA000081G1L	1.0(A00)
<div style="text-align: center;">DELL CONFIDENTIAL/PROPRIETARY</div> <div style="display: flex; justify-content: space-between; align-items: center;"> <div style="border: 1px solid black; padding: 5px; font-size: 0.8em;"> PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT. </div> <div style="text-align: right;"> <div style="border: 1px solid black; padding: 5px; margin-top: 5px;"> Compal Electronics, Inc. Title: EE P.I.R (5/6) Size: Document Number LA-C451P Rev. 1.0 Date: Friday, September 25, 2015 Sheet 60 of 60 </div> </div> </div>							